(Set-1)

B.Tech - 4th Digital Electronics Circuits

Full Marks: 70

Time: 3 hours

Q. No. 1 is compulsory and answer any five from the rest

The figures in the right-hand margin indicate marks

1. Answer the following questions:

 2×10

- (a) What is the utility of Gray code?
- (b) Realise a JK FF to a T FF?
- (c) Determine the values of A, B, C and D that make the sum term $\overline{A} + B + \overline{C} + D$ equal to zero.
- (d) Which type of gate can be used to add two bits?
- (e) The bit sequence 0010 is serially entered

(Turn Over)

- (right-most bit first) into a 4-bit parallel out shift register that is initially clear. What are the Q outputs after two clock pulses?
- (f) When used with an IC, what does the term "QUAD" indicates?
- (g) Convert the fractional binary number 0000.1010 to decimal.
- (h) How many flip-flops are required to make a MOD-32 binary counter?
- (i) A type of digital circuit technology that uses bipolar junction transistors is _____
- (j) Why does the TTL family use a totem-pole circuit on the output?
- 2. Obtain the simplified expressions for the following equations:
 - (a) $F(x,y,z) = \sum (0,1,4,5)$
 - (b) $F(A,B,C,D) = \pi(0,1,2,3,4,10,11)$
 - (c) $F(w,x,y,z) = \sum (1,3,5,7,13,15)$

3. (a) Implement the following function with MUX.

$$F(A,B,C,D) = \Sigma(0,1,3,4,8,9,15)$$
 5

(b) Given a Boolean equation

$$Y = A'BC'D + A'BCD' + AB'CD'$$

show the simlified NAND-NAND circuit for the above equation.

- 4. (a) Draw a circuit for BCD to excess 3 code converter.
 - (b) Draw a suitable TTL LED driver.
- 5. (a) Implement a full adder circuit with multiplexers.
 - (b) A combinational circuit is defined by the following three functions:

$$F_1 = x'y' + xyz', F_2 = x' + y', F_3 = xy + x'y'.$$

Design the circuit with a decoder and external gates.

5

6.	(a)	What is a master slave flip flop? Draw and explain the logic diagram of master slave D flip flop. Use NAND gates only.	5
	(b)	Draw the diagram of a positive edge triggered 4-bit binary ripple up counter using flip flops. Explain its operation using timing diagram.	5
7.	(a)	Design a state diagram for a 3-bit binary up counter and derive its state table and draw its logic circuit diagram.	5
	(b)	The content of a 4-bit shift register is 1100. If the content of a 4 bit shift register is 1100. If the register is shifted 8 times to the right with a serial input 11010010. Explain its operation by showing the content of the register after each shift.	
8.	Write short notes on the following (any three): 10		
	(i)	Decade Counter	
	(ii)	Combinational circuits	
	(iii) Master Slave Flip Flop	
	(iv) Full adder using Half adder	
	(v)	CMOS Logic Circuits.	