VEER SURENDRA SAI UNIVERSITY OF TECHNOLOGY: BURLA
DEPARTMENT OF ELECTRONICS & TELECOMMUNICATION ENGINEERING
Course Structure & Curriculum for M.Tech in "*VLSI SIGNAL PROCESSING"*

First semester:-

Course Code	Subject	L	T	P	C
	Analog and Mixed Mode Signal Design	3	1	0	4
	Digital VLSI Design	3	1	0	4
	VLSI Technology	3	1	0	4
	Semiconductor Device Modeling	3	1	0	4
	Elective-I (Any one from Group-I)	3	1	0	4
	VLSI Design Laboratory-I	0	0	3	2
	VLSI Technology Laboratory	0	0	3	2
	Seminar-I	0	0	3	2
	Comprehensive Viva Voce-I				2
	Total =	15	5	9	28

Second semester:-

Course Code	Subject	L	T	P	C
	HDL and High Level VLSI Design	3	1	0	4
	VLSI Signal Processing	3	1	0	4
	VLSI Testing	3	1	0	4
	Elective-II (Any one from Group-II)	3	1	0	4
	Elective-III (Any one from Group-III)	3	1	0	4
	VLSI Design Laboratory-II	0	0	3	2
	Advanced Simulation Laboratory	0	0	3	2
	Seminar-II	0	0	3	2
	Comprehensive Viva Voce-II				2
	Total =	15	5	9	28

Third Semester:-

Course Code	Subject	L	T	P	C
	Dissertation Interim Evaluation				10
	Comprehensive Viva -Voce				3
	Seminar on Dissertation				2
				Total=	15

Fourth Semester:-

Course Code	Subject	L	T	P	C
	Dissertation Open Defense				5
	Dissertation Final Evaluation				20
				Total=	25
				Grand Total =	96

Group-I (In first semester)
Advanced Digital Signal Processing
Computational Techniques in Microelectronics
FPGA Based DSP Design
Advanced Computer Architecture
Information Theory and Coding

Group-II (In second semester)
MEMS & IC Design
Design with ASICS
Programmable DSP Architecture and Applications
Digital Image Processing
Physical Design Automation

Group-III (In second semester)
CMOS RF Circuit Design
Nano Electronics
Embedded System
Low Power VLSI Design
SoC (System on Chip) Design

ANALOG AND MIXED MODE VLSI DESIGN :(3-1-0) Credit: 4

UNIT-I

Introduction to Analog IC Design, The Design Flow of Analog ICs, MOSFET Parameters, MOSFET Models, MOS Diode, MOS Capacitors, MOS Switch, Noise in MOSFETs.

UNIT-II

MOS Current Sources and Current Sink Circuits, Voltage and Current Reference Circuits, MOS Gain Stages, Source Followers, Amplifiers, Differential Amplifiers, Operation Amplifiers, Stability Theory and Compensation in CMOS Operational Amplifiers.

UNIT-III

OpAmp Design Techniques and Practical Consideration in Design of OpAmp, High Performance CMOS OpAmp Design, Design of MOS Comparators, Data Converter Fundamentals, Digital-to-analog Converters, Analog-to-Digital Converters.

UNIT-IV

Switch Capacitor Filters, Mismatch Issues in Analog Layouts, Phase Locked Loops, Introduction to RF IC Design.

Essential Reading:

1. P.E. Allen and D.R. Holberg, *CMOS Analog Circuit Design*, Oxford University Press, 2004.
2. R. Gregorian and G.C. Temes, *Analog MOS Integrated Circuits for Signal Processing*, John Wiley and Sons, 2004.

Supplementary Reading:

1. R.J. Baker, H. W. Li, D. E. Boyce, *CMOS Circuit Design, Layout, and Simulation,* PHI, 2002
2. P.R. Gray, P.J. Hurst, S.H. Lewis and R.G.Meye, *Analysis and Design of Analog Integrated Circuits*, John Wiley & Sons, Fourth Edition, 2003
3. D.A. Johns and K. Martin, *Analog Integrated Circuit Design*; John Wiley and Sons, 2004
4. B. Raza; *Design of Analog CMOS Integrated Circuits*, Tata McGraw-Hill, 2002
5. M. Ismail and Terri Fiez, *Analog VLSI*, McGraw Hill, 1994

DIGITAL VLSI DESIGN: (3-1-0) Credit: 4

UNIT-I

Introduction to MOSFETs: Fabrication and Modeling (Designer's View -point), MOS Inverter: Static and Switching Characteristics; MOS Capacitor; Resistivity of Various Layers, Symbolic and Physical Layout Systems -- MOS Layers, Stick/Layout Diagrams; Issues of Scaling.

UNIT-II

Combinational MOS Logic Circuits: Pass Transistors/Transmission Gates; Primitive Logic Gates; Complex Logic Circuits, Sequential MOS Logic Circuits: Latches and Flip-flops, Dynamic Logic Circuits; Clocking Issues, Rules for Clocking. Performance Analysis.

UNIT-III

CMOS Subsystem Design; Data Path and Array Subsystems: Addition / Subtraction, Comparators, Counters, Coding, Multiplication and Division.

UNIT-IV

SRAM, DRAM, ROM, Serial Access Memory, Context Addressable Memory.

Essential Reading:

1. J.M Rabey, A. Chandrakasan and B.Nicolic, *Digital Integrated Circuits: A design Prespective*, Second Edition, Pearson/PH, 2003 (Cheap Edition)

Supplementary Reading:

1. J.P Uyemura, *Introduction to VLSI Circuits and Systems*, Wiley, 2001
2. W. Wolf, *Modern VLSI Design: Systems-on Chip Design*, Third Edition, Pearson/PH,2002 (Cheap Edition)
3. R. L. Geiger, P.E. Allen and N.R. Strader, *VLSI Techniques for Analog and Digital Circuits*, McGraw-Hill, 1990

VLSI TECHNOLOGY :(3-1-0) Credit: 4

UNIT-I

Electron Grade Silicon. Crystal Growth. Wafer Preparation. Vapour Phase and Molecular Beam Epitaxy. SOI. Epitaxial Evaluation. Oxidation Techniques, Systems and Properties. Oxidation Defects. Optical, Electron, X-Ray and Ion Lithography Methods.

UNIT-II

Plasma Properties, Size, Control, Etch Mechanism, Etch Techniques and Equipments. Deposition Process and Methods. Diffusion in Solids. Diffusion Equation and Diffusion Mechanisms. Ion Implantation and Metallization.

UNIT-III

Process Simulation of Ion Implementation, Diffusion, Oxidation, Epitaxy, Lithography, Etching and Deposition.

UNIT-IV

NMOS, CMOS, MOS Memory and Bipolar IC Technologies. IC Fabrication. Analytical Techniques, Assembly Techniques and Packaging of VLSI Devices.

Essential Reading:

1. S.M. Sze, *VLSI Technology* (2/e), McGraw Hill, 1988
2. W. Wolf, *Modern VLSI Design*, (3/e), Pearson, 2002
3. S.K. Gandhi, *VLSI Fabrication Principle*, John Willey & Sons

SEMICONDUCTOR DEVICE MODELING :(3-1-0) Credit: 4

UNIT-I

PN Junction Diode and Schottky Diode: DC Current Voltage Circuits, Static Model, Large Signal Model, Small signal Model, Schottky Diode and its Implementation in SPICE 2, Temperature and Area Effect on the Diode Model Parameters, SPICE3, HSPICE & PSPICE Models.

UNIT-II

BJT: Transistor Conversion and Symbols, Ebers-Moll Static, Large Signal and Small Signal Models, Gummel-Poon Static, Large Signal Models, Temperature and Area Effect on the BJT Parameters, Power BJT Models, SPICE3, HSPICE & PSPICE Models
JFET: Static Model, Large Signal Model, Small signal Model and its Implementation in SPICE 2, Temperature and Area Effect on the JFET Model Parameters, SPICE3, HSPICE & PSPICE Models.

UNIT-III

Metal Oxide Semiconductor Transistor (MOST): Structure and Operating Regions of the MOST, Level-1 and Level-2 Static Models, Level-1 and Level-2 Large-Signal Models, Comment on the Three Models, The Effect of Series Resistance, Small-Signal Models, The Effect of Temperature on the MOST Model Parameters, BSIM1 & BSIM2 Models, SPICE3, HSPICE & PSPICE Models.

UNIT-IV

Noise and Distortion: Noise, Distortion in MOSEFT, ISFET, THYRISTOR.

Essential Reading:

1. G. Massobrio and P.Antognetti, *Semiconductor Device Modeling by SPICE*, Second Edition, McGraw Hill, 1993

Supplementary Reading:

2. N. Dasgupta and A. Dasgupta, *Semiconductor Device Modeling,* PHI Publication

VLSI DESIGN LABORATORY-I: (0-0-3) Credit: 2

(The following experiments need to be carried out using HDL Simulation Tools)

1. Design a full adder using dataflow modeling.
2. Design a full adder using half-adder.
3. Design a half adder.
4. Design a 4-bit adder -cum-sub tractor using:
   4:1 MUX using the following:
   (a) Dataflow
   (b) Using when else
   (c) Structural modeling using 2:1 MUX
   (d) Behavioral modeling using
   (i) Case statement
   (ii) If else statement
   (e) Mixed style of modeling (use structural, behavioral, dataflow)
5. Design a decoder (3: 8) and Encoder (Gray to Binary).
6. Design a BCD to 7-Segment Decoder.
7. Interface the 2-bit adder with 7-segment display.
8. Design 4-bit Even/Odd parity checker & generator.
9. Design of Flip-Flops:
   (a) S-R Flip Flop (b) J-K Flip Flop (c) D Flip Flop (d) T Flip Flop
10. (a) Design of counters:
    (i) 4-bit up counter (use asynchronous reset)
    (ii) 4-bit down counter (use synchronous reset)
    (iii) 4-bit up/down counters
    (iv) Decade counter
    (b) Design of Shift Registers:
    (i) Serial-in serial-out
    (ii) Serial-in parallel-out
    (c) Design the following using Generics
    (i) Generic Decoder
    (ii) Generic Parity
    (iii) Detector Generic parity generator
11. Design of a simple Microprocessor Data Path and Control Path using VHDL modeling

VLSI TECHNOLOGY LABORATORY: (0-0-3) Credit: 2

ADVANCED DIGITAL SIGNAL PROCESSING: (3-1-0) Credit: 4

UNIT-I

Multirate Digital Signal Processing: Introduction, Decimation by a Factor D, Interpolation by a Factor I, Sampling Rate Conversion by Rational Factor I/D, Filter Design and Implementation for Sampling-Rate, Multistage Implementation of Sampling Rate Conversion, Sampling Rate Conversion of Band Pass Signal, Application of Multi Rate Signal Processing: Design of Phase Shifters, Implementation of Narrowband Low Pass Filters. Implementation of Digital Filter Banks. Filter Bank and Sub band Filter Applications.

UNIT-II

Linear Prediction and Optimum Linear Filters: Innovations Representation of a Stationary Random Process, Forward and Backward Linear Prediction, Solution of the Normal Equations, Properties of the Linear Prediction-Error Filters, AR Lattice and ARMA Lattice- Ladder Filters, Wiener Filter for Filtering and Prediction: FIR Wiener Filter, Orthogonality Principle in Linear Mean-Square Estimation.

UNIT-III

Power Spectrum Estimation: Estimation of Spectra from Finite-Duration Observation of Signals, Non Parametric Method for Power Spectrum Estimation: Bartlett Method, Blackman and Turkey Method, Parametric Method for Power Estimation: Yuke-Walker Method, Burg Method, MA Model and ARMA Model. Higher Order Statics (HOS): Moments, Cumulants, Blind Parameters and Order Estimation of MA & ARMA Systems-Application of Higher Order Statistics.

UNIT-IV

Adaptive Signal Processing: Least Mean Square Algorithm, Recursive Least Square Algorithm, Variants of LMS Algorithm: SK-LMS, N-LMS, FX-LMS. Adaptive FIR & IIR Filters, Application of Adaptive Signal Processing: System Identification, Channel Equalization, Adaptive Noise Cancellation, Adaptive Line Enhancer.

Essential Reading:

1. J.G. Proakis and D.G. Manolakis, *Digital Signal Processing*, Third Edition, Prentice Hall
2. B. Widrow and Stern, *Adaptive Signal Processing*
3. Haykins, *Adaptive Filter,* PHI

COMPUTATIONAL TECHNIQUES IN MICRO-ELECTRONICS:

(3-1-0) Credit: 4

UNIT-I

Linear and Non-Linear Circuit Simulation Techniques- Algorithms and Computational Methods; Transient Analysis; Frequency Domain Analysis.

UNIT-II

Moment Methods; Sensitivity Analysis, Timing Simulation. Numerical Solution of Differential Equations- FEM, FVM and FDM, Grid Generation, Error Estimates, Transient and Small Signal Solutions, Applications to Device and Process Simulation.

UNIT-III

Introduction to VHDL Modeling. Layout Algorithms, Yield Estimation Algorithms. Symbolic Analysis and Synthesis of Analog ICs.

UNIT-IV

Introduction to Physical Design, Part Training Algorithms, Algorithms for Placement and Floor Planning, Global Routing And Detailed Routing.

TEXT BOOKS:

1. L.O.CHUA AND P.M.LIN "*Computer Aided Analysis of Electronics Circuits: Algorithms and Computational Techniques*"., Prentice –Hall 1975.
2. L.PALLAGE, R.ROHRER ANDC.VISWESWARAIAH, "*Electronics Circuits and Simulation Methods"*, Mc. Graw Hall, 1995.
3., NAVEED SHEWANI, "*Algorithms for VLSI Physical Design Automation*", Kluwer Academic, 1993

FPGA – BASED DSP DESIGN :(3-1-0) Credit: 4

UNIT-I

Multirate Signal Processing- Decimation and Interpolation, Spectrum of Decimated and Interpolated Signals, Polyphase Decomposition of FIR Filters and Its Applications to Multirate DSP.Sampling Rate Converters, Sub-Band Encoder. Filter Banks-Uniform Filter Bank. Direct and DFT Approaches.

UNIT-II

Introduction to ADSL Modem, Discrete Multitone Modulation and Its Realization Using DFT. QMF. Short Time Fourier Transform Computation of DWT Using Filter Banks. Implementation and Verification on FPGAs. DDFS- ROM LUT Approach. Spurious Signals Jitter. Computation of Special Functions Using CORDIC.Vector and Rotation Mode of CORDIC. CORDIC Architectures. Implementation and Verification on FPGAs.

UNIT-III

Block Diagram of a Software Radio. Digital Down Converters and Demodulators. Universal Modulator and Demodulator Using CORDIC. Incoherent Demodulation - Digital Approach for I and Q Generation, Special Sampling Schemes. CIC Filters. Residue Number System and High Speed Filters Using RNS. Down Conversion Using Discrete Hilbert Transform. Undersampling Receivers, Coherent Demodulation Schemes.

UNIT-IV

Speech Coding- Speech Apparatus. Models of Vocal Tract. Speech Coding Using Linear Prediction. CELP Coder. An Overview of Waveform Coding. Vocoders. Vocoder Attributes. Block Diagrams of Encoders and Decoders of G723.1, G726, G727, G728 and G729.

Essential Reading:

1. J. H. Reed, *Software Radio,* Pearson, 2002.
2. U. Meyer – Baese, *Digital Signal Processing with FPGAs*, Springer, 2004

Supplementary Reading:

1. Tsui, *Digital Techniques for Wideband receivers*, Artech House, 2001.
2. S. K. Mitra, *Digital Signal processing*, McGrawHill, 1998

ADVANCED COMPUTER ARCHITECTURES: (3-1-0) Credit: 4

UNIT-I

Introduction: Performance Evaluation – Flynn's Classification – Different Architectural Tracks: RISC & CISC, Control Flow and Data Flow - Sub and Super Scalar Architectures. Pipe-Lining: Linear and Non-Linear Pipelines – Multifunction Pipes – Design of Pipe Lined Processors - Pipeline Hazards – Instruction Scheduling – Dynamic Scheduling – Score Boarding and Tomosulo's Algorithm – Interrupts in Pipeline Processors .Review of Memory Subsystem – Interleaved Memory - Access Methods: C - Access – Virtual Memory.

UNIT-II

Array Processors and Associate Processors. Vector Processing - Basic Ideas – Pipe Lining in Vector Processors – Vector Chaining – Vector Instruction Example CRAY X-MP. Multiprocessor System – Basic Ideas – Interconnection Networks – Instruction Primitives – Maintaining Memory Consistency – Cache Coherency Problems – Virtual Address Cache and Physical Address Cache – Cache Coherence Protocols - Shared Memory Multiprocessors – Consistency Models Weak and Sequential .

UNIT-III

Introduction to Multi Threaded Architecture - Introduction to Data Flow Computers.

UNIT-IV

I/O Subsystem – I/O Processors- Disk Arrays I/O Strategy and Intelligence – Improving Data Rate by Software - Improving Data Rate by Hardware – Shadowing, Striping and Raids.

Essential Reading:

1. Kai Hwang and F.A. Briggs, *Computer Architecture and Parallel Processing*, McGraw Hill Publications
2. Kai Hwang, *Advanced Computer Architecture-Parallelism, Scalability, Programmability*, McGraw Hill, 1993
3. J. Hennessy and D.Patterson, *Computer Architecture, A quantitative approach*, MorgonKaufman, 1993
4. Hockey Jesshope, *Parallel Computer 1 & 2*, Adam Hilgs
5. Herald Stone, *High Performance Computer Architecture*, IEEE Computer Magazine
6. *IEEE Micro.*
7. Papers from International symposia on Computer Architecture (ICSA)

INFORMATION THEORY AND CODING: (3-1-0) Credit: 4

UNIT-I

Information Theory and Source Coding: Introduction to Information Theory, Uncertainty and Information, Average Mutual Information and Entropy, Information Measures for Continuous Random Variables, waveform sources. Amplitude Quantizing: quantizing noise, uniform quantizing, non-uniform quantizing. Differential Pulse Code Modulation: one-tap prediction, N-tap prediction, delta modulation, sigma delta modulation, sigma delta A-to-D convertor(ADC), sigma delta D-to-A convertor(DAC). Block coding: vector quantizing, Transform Coding: quantization for transform coding, Sub-band Coding. Source Coding for Digital Data: properties of codes, Huffman codes, Run-length codes.

UNIT-II

Waveform coding: Antipodal and Orthogonal signals, Orthogonal and Biorthogonal codes, waveform coding system example, Types of error control: Terminal connectivity, automatic repeat request. Structured Sequence: Channel models, Channel capacity, Channel coding, Information Capacity Theorem, The Shannon Limit, Introduction to Error correcting codes, code rate & redundancy, parity check codes: Single parity check code, Rectangular code. Linear Block codes: vector spaces, vector subspaces, A(6,3) linear block code example, Generator matrix, systematic linear block codes, parity-check matrix, syndrome testing, error correction , Decoder implementation

Error Detecting & Correcting Capability: weight & distance of binary vectors, minimum distance of linear code, error detection & correction, visualization of a 6-tuple space, erasure correction. Usefulness of Standard Array: estimating code capability, an (n, k) example, designing the (8,2) code, error detection vs. error correction trade-off

Cyclic Codes: algebraic structures of cyclic code, binary cyclic code properties, encoding in systematic form, circuit for dividing polynomial, systematic encoding with an (n-k)-stage shift register, error detection with an (n-k)-shift register. Well-Known Block Codes: Hamming codes, extended Golay code, BCH codes.

UNIT-III

Convolutional Encoding, Convolutional Encoder Representation: connection representation, state representation & the state diagram, the tree diagram, the trellis diagram. Formulation of the Convolutional Decoding Problem: maximum likelihood decoding, channel models: hard versus soft decisions, Viterbi Convolutional Decoding Algorithm, an example of viterbi convolutional decoding, decoder implementation, path memory and synchronization. Properties of Convolutional Codes: distance properties of convolutional codes, systematic & non-systematic convolutional codes, catastrophic error propagation in convolutional codes, performance bounds for convolutional codes, coding gain, based known convolutional codes, convolutional code rate trade-off, soft-decision viterbi decoding. Other Convolutional Decoding Algorithms: sequential decoding, comparisons & limitations of viterbi & sequential decoding, feedback decoding.

UNIT-IV

Reed-Solomon Codes: Reed-Solomon Error Probability, Why R-S codes perform well against burst noise, R-S performance as a function of size, redundancy, and code rate. Interleaving & Concatenated Codes: Block interleaving, Convolutional interleaving, concatenated codes. Coding & Interleaving Applied to CD Digital Audio System: CIRC encodings, CIRC decoding, interpolation & muting. Turbo Codes: turbo code concepts, log-likelihood algebra.

Essential Reading:

1. Bernard Sklar, *Digital Communications - Fundamentals and Applications*, 2nd Edition, Person Education
2. Ranjan Bose, *Information Theory, Coding & Cryptography*, Tata Mc Graw Hill
3. Simon Haykin, *Digital Communications*, Wiley Edition
4. J.G.Proakis, *Digital Communications*, 3rd Edition, Mc Graw Hill

HDL AND HIGH LEVEL VLSI DESIGN: (3-1-0) Credit: 4

UNIT-I

Basic Concepts of Hardware Description Languages., Hierarchy, Concurrency, Logic and Delay Modeling, Structural, Data-Flow and Behavioral Styles of Hardware Description, Architecture of Event Driven Simulators, Syntax and Semantics of VHDL, Variable and Signal Types, Arrays and Attributes, Operators, Expressions and Signal Assignments, Entities, Architecture Specification and Configurations, Component Instantiation, Concurrent and Sequential Constructs, Use of Procedures and Functions, Examples of Design Using VHDL, Synthesis of Logic From Hardware Description .

UNIT-II

CMOS Process and Masking Steps: Concept of Lambda, Design Rules, Layer Properties and Parasitic Estimation, Sheet Resistance, U Cg, Capacitance Ratio for Layers, Concept of Tau, Quick Estimation of Delays. Design of Buffers and I/O Pads, CMOS Logic Design Styles and Their Comparison, CMOS Logic Design Styles and Their Comparison (Continued), From Specifications to Silicon.

UNIT-III

Abstraction Levels in VLSI Design; Adder Architectures, Multiplier Architectures, Counter Architectures, ALU Architectures. Latches, Flip-Flops, Registers and Register Files. PLA Design, Gate Array Approach, Standard Cell Approach. Moore and Mealy Machines, PLA-Based Implementation, Random Logic Implementation. Micro-Programmed Implementation (ROM-Based Implementation).

UNIT-IV

SRAM Cell, Different DRAM Cells, Arraying of Cells, Address Decoding, Read / Write Circuitry, Sense Amplifier Design, ROM Design. Clock Skew, Clock, Distribution and Routing, Clock Buffering, Clock Domains, Gated Clock, Clock Tree. Concept of Logic Hazards.

Essential Reading:

1. C. H. Roth, *Digital Systems Design Using VHDL*, Thomson Publications, Fourth

Edition, 2002

2. V. A. Pedroni, *Circuit Design with VHDL*, MIT Press/PHI, 2004. (Cheap Edition)
3. Edward J. McClusky, *Logic Design Principles,*

Supplementary Reading:

1. Z. Navabi, *Verilog Digital System Design*, Second Edition, Tata McGraw-Hill, 2008.
2. R. C. Cofer and B. F. Harding, *Rapid System Prototyping with FPGAs: Accelerating the Design Process*, Elsevier/Newnes, 2005.

VLSI SIGNAL PROCESSING :(3-1-0) Credit: 4

UNIT-I

Pipeling and Parallel Processing: Introduction, Pipeling of FIR Digital Filters, Parallel Processing. Pipelining and Parallel Processing for Low Power. Retiming: Introduction, Definition and Properties, Solving System of Inequalities, Retiming Techniques.

UNIT-II

Unfolding: Introduction an Algorithms for Unfolding, Properties of Unfolding, Critical Path, Unfolding and Retiming Application of Unfolding. Folding: Introduction to Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding in Multirate Systems.

UNIT-III

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations Containing Delays.

UNIT-IV

Fast Convolution: Introduction, Cook, Toom Algorithm, Winogard Algorithm, Iterated Convolution, Cyclic Convolution, Design of Fast Convolution Algorithm by Inspection.

Essential Reading:

1. Keshab K. Parhi. *VLSI Digital Signal Processing Systems*, Wiley-Inter Sciences, 1999
2. Mohammed Ismail, Terri, Fiez, *Analog VLSI Signal and Information Processing*, McGraw Hill, 1994.
3. Kung. S.Y., H.J. While house T.Kailath, *VLSI and Modern singal processing*, Prentice Hall, 1985.
4. Jose E. France, Yannis Tsividls, *Design of Analog Digital VLSI Circuits for Telecommunications and Signal Processing*' Prentice Hall, 1994.

VLSI TESTING :(3-1-0) Credit: 4

UNIT-I

Combinational ATPG. Current Sensing Based Testing. Classification of Sequential ATPG Methods. Fault Collapsing and Simulation, Universal Test Sets. Pseudo-Exhaustive and Iterative Logic Array Testing. Clocking Schemes for Delay Fault Testing, Testability Classifications for Path Delay Faults, Test Generation and Fault Simulation for Path and Gate Delay Faults.

UNIT-II

CMOS Testing: Testing of Static and Dynamic Circuits. Fault Diagnosis: Fault Models for Diagnosis, Cause-Effect Diagnosis, Effect-Cause Diagnosis.

UNIT-III

Design for Testability: Scan Design, Partial Scan, Use of Scan Chains, Boundary Scan, DFT for Other Test Objectives.

UNIT-IV

Built-In Self-Test: Estimation of Test Length, Test Points to Improve Testability, Analysis of Aliasing in Linear Compression, BIST Methodologies, BIST for Delay Fault Testing. Testing of Analog and Mixed Signal Circuits.

Essential Reading:

1. N. Jha & S.D. Gupta, *Testing of Digital Systems, Cambridge*, 2003.
2. M. Abramovici et.al., *Digital System Testing and Testable Design*, Computer Science Press, 1990
3. M.L.Bushnell & V.D.Agarwal, *Essentials of Electronic Testing for Digital, Memory and Mixed signal VLSI circuits*, Kluwer, 2000

Supplementary Reading:

1. P.K.LALA, *Digital Circuit Testing and Testability*, Academic Press, 1999.
2. P.K.LALA, *Self checking and Fault-tolerant Digital Design*, Academic Press, 1999.

VLSI DESIGN LABORATORY-II: (0-0-3) Credit: 2

(The following experiments need to be carried out using Mentor Graphics and Cadence Digital and Analog Design environments)

1. Design of different Current mirror circuits
2. Design of Reference Circuits
3. Design of Amplifiers
4. Design of Differential Amplifiers
5. Design of CMOS OP-AMP
6. Design of Comparators
7. Design of flash ADC
8. Design of SAR ADC
9. Design of Switch Capacitor Filter
10. Implementation of VCO by Ring Oscillator design
11. Design of DPLL
12. Design of ADPLL

ADVANCED SIMULATION LABORATORY: (0-0-3) Credit: 2

(The following experiments need to be carried out using MATLAB)

1. Signal Decomposition using Multi Resolution Techniques.
2. Wavelet Coding Techniques
3. Spectral Estimation Using Parametric Method
4. Higher Order Statistics of a Signal
5. PCA/ICA Analysis

MEMS AND IC DESIGN :(3-1-0) Credit: 4

UNIT-I

Overview of CMOS Process in IC Fabrication, MEMS System-Level Design Methodology, Equivalent Circuit Representation of MEMS, Signal-Conditioning Circuits, and Sensor Noise Calculation.

UNIT-II

Pressure Sensors with Embedded Electronics (Analog/Mixed Signal): Accelerometer with Transducer, Gyroscope, RF MEMS Switch with Electronics, Bolo Meter Design.

UNIT-III

RF MEMS

UNIT-IV

Optical MEMS

Essential/Supplementary Reading:

1. Gregory T.A. Kovacs, *Micromachined Transducers Sourecbook*, McGraw-Hill Inc., 1998
2. Stephen D. Senturia, *Microsystem Design*, Kluar Publishers, 2001
3. Nadim Maluf, *an Introduction to Microelectromechanical Systems Engineering*, Artech House, 2000
4. M.H. Bao, *Micro Mechanical Transducers*, Volume 8, Handbook of Sensors and Actuators, Elsevier, 2000
5. Masood Tabib-Azar, *Microactuators*, Kluwer, 1998
6. Ljubisa Ristic, Editor, *Sensor Technology and Devices*, Artech House, 1994
7. D. S. Ballantine, et. al., *Acoustic Wave Sensors*, Academic Press, 1997
8. H. J. De Los Santos, *Introduction to Microelectromechanical (MEM) Microwave Systems*, Artech, 1999
9. James M.Gere and Stephen P. Timoshenko, *Mechanics of Materials*, 2nd Edition, Brooks/Cole Engineering Division, 1984

DESIGN WITH ASICS :(3-1-0) Credit: 4

UNIT-I

Types of ASICs. ASIC Design Flow. Programmable ASICs. Anti Fuse, SRAM, EPROM, EEPROM Based ASICs. Programmable ASIC Logic Cells and I/O Cells. Programmable Interconnects. An Overview of Advanced FPGAs and Programmable SOCs: Architecture and Configuration of Spartan and Virtex FPGAs. Apex and Cyclone FPGAs. Virtex PRO Kits and Nios Kits. OMAP.

UNIT-II

ASIC Physical Design Issues. System Partitioning, Interconnect Delay Models and Measurement of Delay. ASIC Floor Planning, Placement and Routing.

UNIT-III

Design Issues in SOC. Design Methodologies. Processes and Flows. Embedded Software Development for SOC. Techniques for SOC Testing. Configurable SOC. Hardware/Software Co-design. High Performance Algorithms for ASICs/ SOCs.

UNIT-IV

SOC Case Studies- DAA and Computation of FFT and DCT. High Performance Filters Using Delta-Sigma Modulators. Case Studies: Digital Camera, Bluetooth Radio/Modem, SDRAM and USB Controllers.

Essential Reading:

1. M.J.S. Smith: *Application Specific Integrated Circuits,* Pearson, 2003

Supplementary Reading:

1. K.K.Parhi, *VLSI Digital Signal Processing Systems,* John-Wiley, 1999

PROGRAMMABLE DSP ARCHITECTURE AND APPLICATIONS:

(3-1-0) Credit: 4

UNIT-I

Introduction to digital signal processing: The Sampling Theorem and Digital Signal Sequences, Frequency Response and FIR/ IIR Filters, DFT and FFT, Computer Based Tools for DSP Analysis and Design. Architectural Requirements of a DSP Device: Architectures and hardware to implement DSP operations and algorithms, Comparison of various DSP architectures in use. Programmable DSP Devices**:** Architectural Analysis of a DSP Device, The Instruction Set and the Addressing Modes, Writing Assembly Code for Applications.

UNIT-II

DSP Implementation Tools**:** DSP Software Development Tools: Compiler, Assembler, Linker, Simulator, and Debugger. Software Implementations of DSP Algorithms**:** Assembly Code Implementations: FIR Filters, IIR Filters, Interpolation Filters, Decimation, Filters, PID Controllers, Adaptive Filters, and Nonlinear Operations. Interfacing Serial Converters to a Programmable DSP Device**:** Synchronous Serial Interface between the DSP and an AIC, A Multi-channel Buffered Serial Port (MCBSP) ,The MCBSP Programming, An Analog Interface Circuit (AIC).

UNIT-III

Computational Accuracy in DSP Implementations**:** The DSP System Model, Quantization, Truncation, Rounding, Overflow, and Saturation Errors in DSP Implementations.

UNIT-IV

Software Implementations of FFT Algorithms**:** Spectrum Analysis, Interfacing Memory and Parallel I/O Peripherals to Programmable DSP Devices: Memory Interfacing, A/D and D/A Interfacing.

Essential Reading:

1. Singh, A. and Srinivasan, S., "*Programmable DSP Architecture and Applications"* Thomson, 2004.

Supplementary Reading:

1. Higgins, R.J. "*Digital Signal Processing in VLSI*", Prentice-Hall, 1990.
2. Strum, R., and Kirk, D., "*First Principles of Discrete Systems and Digital Signal Processing*", Addison Wesley, 1988.
3. Bateman, A. and Yates, W. "*Digital Signal Processing Design"*, Computer Science Press, 1989.
4. Texas Instrument "*Digital Signal Processing Applications with the TMS320 Family*", Prentice-Hall, 1988.
5. Texas Instruments "*TMS320C5X User's Guide*", 1990.
6. El-Sharkawy, M.,"*Real Time Digital Signal Processing with Motorola's DSP56000 Family"*, Prentice- Hall, 1990.
7. Embree, P.M. and Kimble, B.,"*C Language Algorithms for Digital Signal Processing"*, Prentice-Hall, 1991.
8. Texas Instruments, "Linear Circuits: *Data Conversion, DSP Analog Interface, and Video Interface*", 1992.
9. Chassaing, R. and Horning, D. W., "*Digital Signal Processing with the TMS320C25*", Wiley, New York, 1990.
10. Chassaing, R. and Horning, D. W., "*Digital Signal Processing with C and the T MS320C30"*, Wiley, New York, 1992.
11. Lapsley, P. etal , "*DSP Processor Fundamentals: Architectures and Features*", IEEE Press, 1997
12. Math Works, "*The Student Edition of MATLAB with DSP Toolbox*", Prentice-Hall, 1992 or later

DIGITAL IMAGE PROCESSING: (3-1-0) Credit: 4

UNIT-I

Digital Image Fundamentals: A Simple Image Model, Sampling and Quantization, Imaging Geometry, Digital Geometry, Image Acquisition Systems, Different Types of Digital Images. Bi-level Image Processing: Basic Concepts of Digital Distances, Distance Transform, Medial Axis Transform, Component Labeling, Thinning Morphological Processing, Extension to Grey Scale Morphology.

UNIT-II

Binarisation and Segmentation of Grey Level Images: Histogram of Grey Level Images, Optimal Thresholding Using Bayesian Classification, Multilevel Thresholding, Segmentation of Grey Level Images, Water Shade Algorithm for Segmentation Grey Level Image.

UNIT-III

Detection of Edges and Lines in 2D Images: First Order and Second Order Edge Operators, Multi-Scale Edge Detection, Canny's Edge Detection Algorithm, Hough Transform for Detecting Lines and Curves, Edge Linking. Images Enhancement: Point Processing, Spatial Filtering, Frequency Domain Filtering, Multi-Spectral Image Enhancement, Image Restoration. Color Image Processing: Color Representation, Laws of Color Matching, Chromaticity Diagram, Color Enhancement, Color Image Segmentation, Color Edge Detection, Color Demosaicing.

UNIT-IV

Image Restoration and Depth Estimation: Registration Algorithms, Stereo Imaging, Computation of Disparity Map. Image Compression: Lossy and Lossless Compression Schemes, Prediction Based Compression Schemes, Vector Quantization, Sub-Band Encoding Schemes, JPEG Compression Standard, Fractal Compression Scheme, Wavelet Compression Scheme.

Essential Reading:

1. A.K.Jain, *Fundamentals of Digital Image Processing,* PHI, 1995
2. Arthur R.Weeks, Jr., *Fundamentals of Electronic Image Processing,* PHI
3. B.Chanda, D.Dutta Majumadar, *Digital Image Processing and Analysis*, PHI
4. Rafael C.Gonzalez, Richard E. Woods, *Digital Image Processing*, Pearson Education.

PHYSICAL DESIGN AUTOMATION :(3-1-0) Credit: 4

UNIT-I

Preliminaries: Introduction to Design Methodologies, Design Automation Tools, Algorithmic Graph Theory, Computational Complexity, Tractable and Intractable Problems. General purpose methods for combinational optimization: Backtracking, Branch And Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu Search, Genetic Algorithms.

UNIT-II

Layout Compaction, Placement, Floor Planning And Routing Problems, Concepts and Algorithms. Modeling and simulation: Gate Level Modeling and Simulation, Switch Level Modeling and Simulation.

UNIT-III

Logic synthesis and verification: Basic Issues and Terminology, Binary-Decision Diagrams, Two-Level Logic Synthesis. High-level synthesis: Hardware Models, Internal Representation of the Input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some Aspects of Assignment Problem, High-Level Transformations.

UNIT-IV

Physical design automation of FPGA'S: FPGA Technologies, Physical Design Cycle for FPGA's, Partitioning and Routing for Segmented and Staggered Models. Physical design automation of MCM'S: MCM Technologies, MCM Physical Design Cycle, Partitioning, Placement - Chip Array Based And Full Custom Approaches, Routing – Maze Routing, Multiple Stage Routing, Topologic Routing, Integrated Pin – Distribution And Routing, Routing And Programmable MCM's.

Essential Reading:

1. NAVEED SHEWANI, "*Algorithms for VLSI Physical Design Automation*", Kluwer Academic, 1993
2. S.H. Gerez, "*Algorithms for VLSI Design Automation*", John Wiley, 1998.
3. S.M. Sait & H. Youssef, "*VLSI Physical Design Automation*", World scientific, 1999.
4. M.Sarrafzadeh, "*Introduction to VLSI Physical Design*", McGraw Hill (IE), 1996

CMOS RF CIRCUIT DESIGN :(3-1-0) Credit: 4

UNIT-I

Introduction to RF Design and Wireless Technology: Design and Applications, Complexity and Choice of Technology. Basic Concepts in RF Design: Nonlinearly and Time Variance, Inter symbol Interference, Random Processes and Noise. Sensitivity and Dynamic Range, Conversion of Gains and Distortion.

UNIT-II

RF Modulation: Analog and Digital Modulation of RF Circuits, Comparison of Various Techniques for Power Efficiency, Coherent and Non-Coherent Detection, Mobile RF Communication and Basics of Multiple Access Techniques. Receiver and Transmitter Architectures. Direct Conversion and Two-Step Transmitters. RF Testing: RF Testing for Heterodyne, Homodyne, Image Reject, Direct IF And Sub Sampled Receivers.

UNIT-III

BJT and MOSFET Behavior at RF Frequencies: BJT and MOSFET Behavior at RF Frequencies, Modeling of the Transistors and SPICE Model, Noise Performance and Limitations of Devices, Integrated Parasitic Elements at High Frequencies and Their Monolithic Implementation

UNIT-IV

RF Circuits Design: Overview of RF Filter Design, Active RF Components & Modeling, Matching and Biasing Networks. Basic Blocks in RF Systems and Their VLSI Implementation, Low Noise Amplifier Design in Various Technologies, Design of Mixers at GHz Frequency Range, Various Mixers- Working and Implementation. Oscillators- Basic Topologies VCO and Definition of Phase Noise, Noise Power and Trade Off. Resonator VCO Designs, Quadrature and Single Sideband Generators. Radio Frequency Synthesizers- PLLs, Various RF Synthesizer Architectures and Frequency Dividers, Power Amplifier Design, Liberalization Techniques, Design Issues in Integrated RF Filters.

Essential Reading:

1. Thomas H. Lee, *Design of CMOS RF Integrated Circuits*, Cambridge University press, 1998

Supplementary Reading:

1. B. Razavi, *RF Microelectronics*, PHI, 1998
2. R. Jacob Baker, H.W. Li, D.E. Boyce, *CMOS Circuit Design, Layout and Simulation*, PHI, 1998
3. Y.P. Tsividis, *Mixed Analog and Digital Devices and Technology*, TMH, 1996

NANO ELECTRONICS :(3-1-0) Credit: 4

UNIT-I

Introduction: Introduction to Nanoscale Systems, Length Energy and Time Scales, Top Down Approach to Nano Lithography, Spatial Resolution of Optical, Deep Ultraviolet, X-Ray, Electron Beam and Ion Beam Lithography,

UNIT-II

Single Electron Transistors, Coulomb Blockade Effects in Ultra Small Metallic Tunnel Junctions.

UNIT-III

Quantum Mechanics: Quantum Confinement of Electrons in Semiconductor Nano Structures, Two Dimensional Confinement (Quantum Wells), Band Gap Engineering, Epitaxy, Landaeur – Buttiker Formalism for Conduction in Confined Geometries, One Dimensional Confinement, Quantum Point Contacts, Quantum Dots and Bottom Up Approach, Introduction to Quantum Methods for Information Processing.

UNIT-IV

Molecular Techniques: Molecular Electronics, Chemical Self Assembly, Carbon Nano Tubes, Self Assembled Mono Layers, Electromechanical Techniques, Applications in Biological and Chemical Detection, Atomic Scale Characterization Techniques, Scanning Tunneling Microscopy, Atomic Force Microscopy

Essential Reading:

1. Beenaker and Van Houten, *Quantum Transport in Semiconducto Nanostructures in Solid State Physics*, Ehernreich and Turnbell, Academic press, 1991

Supplementary Reading:

1. David Ferry, *Transport in Nano Structures* ,Cambridge University press, 2000
2. Y. Imry, *Introduction to Mesoscopic Physics*, Oxford University press, 1997
3. S. Dutta, *Electron Transport in Mesoscopic Systems*, Cambridge University press, 1995
4. H. Grabert and M. Devoret, *Single Charge Tunneling* ,Plenum press, 1992

EMBEDDED SYSTEM :(3-1-0) Credit: 4

UNIT-I

Introduction: An Embedded System, Processor in The System, Other Hardware Units, Software Embedded into a System, Exemplary Embedded Systems, Embedded System-On-Chip (SOC) and in VLSI Circuit. Devices and Device Drivers: I/O Devices, Timer and Counting Devices, Serial Communication Using The 'I^2C', 'CAN' and Advanced I/O Buses between the Networked Multiple Devices, Host System or Computer Parallel Communication between the Networked I/O Multiple Devices Using the ISA, PCI, PCI-X and Advanced Buses, Device Drivers, Parallel Port Device Drivers in a System, Serial Port Device Drivers in a System, Interrupt Servicing (Handling) Mechanism.

UNIT-II

Software and Programming Concept: Processor Selection for an Embedded System, Memory Selection for an Embedded System, Embedded Programming in C++, Embedded Programming in Java, Unified Modeling Language (UML), Multiple Processes and Application, Problem of Sharing Data by Multiple Tasks and Routines, Inter Process Communication.

UNIT-III

Real Time Operating System: Operating System Services, I/O Subsystems, Network Operating Systems, Real-Time and Embedded System Operating Systems, Need of a Well Tested and Debugged Real-Time Operating System (RTOS), Introduction to Mc/OS-II. Case Studies of Programming with RTOS: Case Study of an Embedded System for a Smart Card.

UNIT-IV

Hardware and Software Co-Design: Embedded System Project Management Embedded System Design and Co-Design Issues in System Development Process, Design Cycle in the Development Phase for an Embedded System, Use of Software Tools for Development of Embedded System, Issues in Embedded System Design.

Essential Reading:

1. Ralf Niemann, Kluwer Academic, *Hardware Software Co-design of Embedded Systems*,
2. Hermann Kopetz, Kluwer Academic, *Design Principles of Distributed Embedded Applications,*
3. Sriram V. Iyer & Pankaj Gupta, *Embedded Real-Time Systems Programming*, TMH.
4. Peter Marwedel *Embedded System Design,* Springer, 2003
5. Wolf, *Embedded System Design*,

LOW POWER VLSI DESIGN :(3-1-0) Credit: 4

UNIT-I

Introduction: Need for Low Power VLSI Chips, Sources of Power Dissipation on Digital Integrated Circuits. Emerging Low Power Approaches, Physics of Power Dissipation in CMOS Devices. Device & Technology Impact on Low Power: Dynamic Dissipation in CMOS, Transistor Sizing & Gate Oxide Thickness, Impact of Technology Scaling, Technology & Device Innovation. Power Estimation, Simulation Power Analysis: SPICE Circuit Simulators, Gate Level Logic Simulation, Capacitive Power Estimation, Static State Power, Gate Level Capacitance Estimation, Architecture Level Analysis, Data Correlation Analysis in DSP Systems, Monte Carlo Simulation. Probabilistic Power Analysis: Random Logic Signals, Probability & Frequency, Probabilistic Power Analysis Techniques, Signal Entropy.

UNIT-II

Low Power Design: Circuit Level; Power Consumption in Circuits. Flip Flops & Latches Design, High Capacitance Nodes, Low Power Digital Cells Library. Logic Level; Gate Reorganization, Signal Gating, Logic Encoding, State Machine Encoding, Pre-Computation Logic.

UNIT-III

Low Power Architecture & Systems: Power & Performance Management, Switching Activity Reduction, Parallel Architecture with Voltage Reduction, Flow Graph Transformation, Low Power Arithmetic Components, Low Power Memory Design. Low Power Clock Distribution: Power Dissipation in Clock Distribution, Single Driver Vs Distributed Buffers, Zero Skew Vs Tolerable Skew, Chip & Package Co Design of Clock Network.

UNIT-IV

Algorithm & Architectural Level Methodologies: Introduction, Design Flow, Algorithmic Level Analysis & Optimization, Architectural Level Estimation & Synthesis.

Essential Reading:

1. Gary K. Yeap, *Practical Low Power Digital VLSI Design*, KAP, 2002
2. Kaushik Roy, Sharat Prasad, *Low-Power CMOS VLSI Circuit Design*, Wiley, 2000

Supplementary Reading:

1. Rabaey, Pedram, *Low power design methodologies,* Kluwer Academic, 1997
2. W. Nebel and J. Mermet, *Low Power Design in Deep Sub-micron Electronics,* Kluwer Academic Publishers, 1997