Course Structure and Curriculum of

Master of Technology in Electronics and Telecommunication Engineering (Specialization: VLSI Signal Processing)

FROM 2019-20 ONWARDS

DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION ENGINEERING

VEER SURENDRA SAI UNIVERSITY OF TECHNOLOGY, ODISHA, BURLA, SAMBALPUR – 768018, INDIA

VISION

To be recognized as a center of excellence in education and research in the field of Electronics and Telecommunication Engineering by producing innovative, creative and ethical Electronics and Telecommunication Engineering professionals for socio-economic upliftment of society in order to meet the global challenges.

MISSION

Electronics and Telecommunication Engineering Department of VSSUT Burla strives to impart quality education to the students with enhancement of their skills to make them globally competitive through:

M1. Maintaining state of the art research facilities to provide enabling environment to create, analyze, apply and disseminate knowledge.

M2. Fortifying collaboration with world class R&D organizations, educational institutions, industry and alumni for excellence in teaching, research and consultancy practices to fulfil 'Make in India' policy of the Government.

M3. Providing the students with academic environment of excellence, leadership, ethical guidelines and lifelong learning needed for a long productive career.

PROGRAM EDUCATIONAL OBJECTIVES

The program educational objectives of M.Tech. in Electronics and Telecommunication Engineering (VLSI Signal Processing) program of VSSUT Burla are to prepare its graduates:

1. To acquire competency in solving real-life problems and to design/develop sustainable and cost-effective products according to the prevailing socio-economic context.
2. To make them enable to excel in their professional career/entrepreneurial skill/research and higher studies.
3. To provide opportunity to work and communicate effectively in a team and to engage in the process of life-long learning.

PEO-MISSION MATRIX

	M1	M2	M3
PEO1	**3**	**1**	**1**
PEO2	**1**	**3**	**2**
PEO3	**2**	**3**	**3**

PROGRAM OUTCOMES for M.Tech. (VLSISP)

PO1	An ability to independently carry out research/investigation and development work to solve practical problems.
PO2	An ability to write and present a substantial technical report/document
PO3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.
PO4	A knowledge to apply appropriate techniques, resources and EDA tools for modelling of specific problem domain.
PO5	Collaborative and multi-disciplinary scientific research back ground to strengthen industry-outcome, based on academics.
PO6	The ability to create and enhancement of higher lifelong learning independently.

Program Specific Outcomes for M.Tech. (VLSISP)

PSO1	To be able to understand the concepts of VLSI Signal Processing and their applications in the field of VLSI technology, electronics circuit design, signal processing, communication/ networking and other relevant areas.
PSO2	To have an ability to apply technical knowledge and usage of modern hardware & software tools related to VLSI Signal processing for solving real world problems.

COURSE STRUCTURE

Semester I

Sl. No.	Core/ Elective	Subject Code	Subject Name	L	T	P	Credits
1	Core-1	MECVP101	Analog CMOS VLSI Design	3	0	0	3
2	Core-2	MECVP102	Advanced Signal Processing	3	0	0	3
3	PE-1		PE-1	3	0	0	3
4	PE-2		PE-2	3	0	0	3
5	Common		Research Methodology & IPR	3	0	0	3
6	Lab-1	MECVP103	VLSI Design Laboratory-I	0	0	3	2
7	Lab-2	MECVP104	VLSI Technology Laboratory	0	0	3	2
8	Audit -1		English for Research Paper Writing				
Total Credits							19

Semester II

Sl. No.	Core/ Elective	Subject Code	Subject Name	L	T	P	Credits
1	Core-3	MECVP201	VLSI Signal Processing	3	0	0	3
2	Core-4	MECVP202	Digital Signal Processor Architecture	3	0	0	3
3	PE-3		PE-3	3	0	0	3
4	PE-4		PE-4	3	0	0	3
5	Common		Term Paper	0	0	4	2
6	Lab-3	MECVP203	VLSI Design Laboratory-II	0	0	3	2
	Lab-4	MECVP204	VLSI Signal Processing Laboratory	0	0	3	2
8	Audit -2		Pedagogy Studies				
Total Credits							18

Semester III

Sl. No.	Core/ Elective	Subject Code	Subject Name	L	T	P	Credits
1	PE-5		PE-5	3	0	0	3
2	OE-1		OE-1	3	0	0	3
3	Minor Project		Dissertation (Phase-I)	0	0	20	10
Total Credits							16

Semester IV

Sl. No.	Core/ Elective	Subject Code	Subject Name	L	T	P	Credits
1	Major Project		Dissertation (Phase-II)	0	0	32	16
Total Credits							16

GRAND TOTAL CREDITS: 19+18+16+16= 69

Program Electives

First Semester			
Program Elective-I		**Program Elective-II**	
Course Code	**Course Name**	**Course Code**	**Course Name**
MVPPE101	Digital CMOS VLSI Design	MVPPE104	VLSI Technology
MVPPE102	Electronic Design Automation	MVPPE105	Semiconductor Device Modelling
MVPPE103	VLSI Algorithm	MVPPE106	JTFA & MRA
Second Semester			
Program Elective-III		**Program Elective-IV**	
MVPPE201	High Level VLSI Design	MVPPE204	VLSI Design Verification & Testing
MVPPE202	RTL Simulation & Synthesis	MVPPE205	Low Power VLSI Design
MVPPE203	CAD of Digital Systems	MVPPE206	Design with ASIC
Third Semester			
Program Elective-V		**Open Electives**	
MVPPE301	RF IC	MVPOE301	Signal Processing
MVPPE302	FPGA Based DSP Design	MPSOE302	Basics of VLSI Engineering
MVPPE303	Physical Design Automation		

Audit course 1 & 2

Sl.No.	Course Code	Subject Name
1.	BCAC1001	English for Research Paper Writing
2.	BCAC1002	Disaster Management
3.	BCAC1003	Sanskrit for Technical Knowledge
4.	BCAC1004	Value Education
5.	BCAC2001	Constitution of India
6.	BCAC2002	Pedagogy Studies
7.	BCAC2003	Stress Management by Yoga
8.	BCAC2004	Personality Development through Life Enlightenment Skills.

First Semester

ANALOG CMOS VLSI DESIGN

SYLLABUS

Module-I (8 hours)

MOS Device and Modeling: The MOS Transistor, Passive Components- Capacitors and Resistors, Integrated Circuit Layout, CMOS Device Modeling- Simple MOS Large Signal Model, Other MOSLargeSignalModelParameters,SmallSignalModeloftheMOS
Transistor, Computer Simulator Models, Subthreshold MOS Model.

Module-II (8hours)

Analog CMOS Sub Circuits: MOS Switch, MOS Diode/Active Resistor, MOS Current Sinks and Sources, Current Mirrors- Current Mirror with Beta Helper, Cascode Current Mirror and Wilson Current Mirror, Voltage and Current References, Bandgap Reference.

Module-III (8 hours)

CMOS Amplifiers: Inverters, Differential Amplifiers,Cascode Amplifiers, Current Amplifiers, Output Amplifiers.

Module-IV (8 hours)

CMOS Operational Amplifiers: Design of Op-Amps,Compensation of OP-Amps, Design of a Two-Stage OP-Amp, Power Supply Rejection Ratio of Two Stage Op-Amp.

Module-V (8 hours)

Comparators: Characterization of a Comparator, Two Stage Open LoopComparators,DiscreteTimeComparators.OtherOpenLoop
Comparators,ImprovingthePerformanceofOpenLoopComparators.

Recommended Books

TEXT BOOKS	1. Philip.E. Allen and Douglas.R. Holberg, "*CMOS Analog Circuit Design*", Oxford University Press, Indian3rd Edition,2012. 2. Paul.R.Gray,Paul.J.Hurst,S.H.LewisandR.G.Meyer,"*AnalysisandDesign of Analog Integrated Circuits"*, Wiley India, Fifth Edition, 2010.
REFERENCE BOOKS	1. 1.R.J. Baker, H. W. Li, D. E. Boyce, "*CMOS Circuit Design, Layout, and Simulation"*, PHI,2002 2. D.A. Johns and K. Martin, "*Analog Integrated Circuit Design*"; Wiley Student Edition, 2013 3. B. Razavi, "*Design of Analog CMOS Integrated Circuits*", Tata McGraw-Hill, 2002.

Course Outcomes:

Upon completion of the course, the students will demonstrate the ability to:

CO1	Know the key subjects of MOSFET large-signal and small signal model to predict the performance of CMOScircuit.
CO2	To visualize how sub circuits and amplifiers are used to design more complex analog circuits, such asop-amp.
CO3	Learn the design procedures of different CMOS amplifiercircuits.
CO4	Designtwostageop-ampwithmethodsofcompensationandtoknowhowuncompensated two stage op-amp acts as open loopcomparator.
CO5	Characterize different comparator circuits and improve theirperformances.

Course Articulation Matrix

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	**3**	**2**	**3**	**3**	**2**	**1**
CO2	**3**	**2**	**3**	**3**	**2**	**1**
CO3	**3**	**2**	**3**	**3**	**2**	**1**
CO4	**3**	**2**	**3**	**3**	**2**	**1**
CO5	**3**	**2**	**3**	**3**	**2**	**1**

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) -: No Correlation

Program Articulation Matrix row for this Course

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
Course	**3**	**2**	**3**	**3**	**2**	**1**

ADVANCED SIGNAL PROCESSING

SYLLABUS

Module-I (8 hours)

Multi-Rate Digital Signal Processing: Introduction, Decimation by A Factor D, Interpolation by A Factor I, Sampling Rate Conversion by Rational Factor I/D, Filter Design and Implementation for Sampling-Rate, Multistage Implementation of Sampling Rate Conversion, Sampling Rate Conversion of Band-Pass Signal, Application of Multi Rate Signal Processing: Design of Phase Shifters, Implementation pf Narrowband Low Pass Filters. Implementation of Digital Filter Banks

Module-II (8hours)

***Linear Prediction and Optimum Linear Filters*:**Innovations Representation of a Stationary Random Process, Forward and Backward Linear Prediction, Solution of The Normal Equations, Properties of The Linear Prediction Error Filters, AR Lattice and ARMA Lattice-Ladder Filters, Wiener Filter For Filtering and Prediction: FIR Wiener Filter, Orthogonality, Principle in Linear Mean-Square Estimation.

Module-III (8 hours)

Power Spectrum Estimation: Estimation of Spectra from Finite- Duration Observation of Signals, Non-Parametric Method for Power Spectrum Estimation: Bartlett Method, Blackman And Turkey Method, Parametric Method for Power Estimation: Yuke-Walker Method, Burg Method, MA Model and ARMA Model. Filter Bankand - Filters and Its Applications.

Module-IV (8 hours)

CMOS Operational Amplifiers: Design of Op-Amps,Compensation of OP-Amps, Design of a Two-Stage OP-Amp, Power Supply Rejection Ratio of Two Stage Op-Amp.AdaptiveSignalProcessingLeastMeanSquareAlgorithm,Recursive Least Square Algorithm, Variants of LMS Algorithm: SK-LMS, N- LMS,FX-LMS.AdaptiveFIR&IIRFilters,ApplicationofAdaptive SignalProcessing:SystemIdentification,ChannelEqualization,Adaptive Noise Cancellation, Adaptive Line Enhancer.

Module-V (8 hours)

HOS- Higher Order Statistics: Definitions and Properties, Moments, Cumulants, Blind Parameters and Order Estimation of MA & ARMA Systems. Application of Higher Order Statistics: Applications to Signal Processing and Image Processing**.**

Recommended Books

TEXT BOOKS	1. J.G. Proakis and D.G. Manolakis, “Digital Signal Processing”, 3rd Edition,PHI.
REFERENCE BOOKS	1. Oppenheim and Schafer, “Digital Signal Processing”, PHI 2. B. Widrow and Stern, “Adaptive Signal Processing”,PHI,1985

Course Outcomes:

Upon completion of the course, the students will demonstrate the ability to:

CO1	Have a more thorough understanding of the relationship between time and frequency domain interpretations.
CO2	Implementations of signal processingalgorithms.
CO3	Be familiar with some of the most important advanced signal processing techniques, including multi-rate processing and time-frequency analysistechniques
CO4	Understanding power spectrum estimationtechniques.
CO5	Understand and be able to implement adaptive signal processing algorithms based on second orderstatistics

Course Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**3**	**2**	**3**	**3**	**2**	**1**
CO2	**3**	**2**	**3**	**3**	**2**	**1**
CO3	**3**	**2**	**3**	**3**	**2**	**1**
CO4	**3**	**2**	**3**	**3**	**2**	**1**
CO5	**3**	**2**	**3**	**3**	**2**	**1**

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) -: No Correlation

Program Articulation Matrix row for this Course

	PO1	PO2	PO3	PO4	PO5	PO6
Course	**3**	**2**	**3**	**3**	**2**	**1**

DIGITAL CMOS VLSI DESIGN

SYLLABUS

Module-I (8 hours)

Introduction to MOSFETs: MOS Inverter, Static and Switching Characteristics, Voltage Transfer characteristics, Noise Margin, RegenerativeProperty,PowerandEnergyConsumption,Stick/Layout Diagrams; Issues of Scaling.

Module-II (8hours)

Combinational MOS Logic Circuits: Pass Transistors, Transmission Gates, Primitive Logic Gates; Complex Logic Circuits.

Module-III (8 hours)

Sequential MOS Logic Circuits: Latches and Flip-flops, Dynamic Logic Circuits; Clocking Issues, Rules for Clocking, Performance Analysis, Logical effort.

Module-IV (8 hours)

CMOS Subsystem Design; Data Path and Array Subsystems: Addition, Subtraction, Comparators, Counters, Coding, Multiplication and Division.

Module-V (8 hours)

Memory Design:SRAM, DRAM, ROM, Serial Access Memory,Content Addressable Memory, Field

Programmable Gate Array.

Recommended Books

TEXT BOOKS	1. Rabey J.M, A. Chandrakasan, and B.Nicolic, "*Digital Integrated Circuits: A design Perspective*", Second Edition, Pearson/PH, 2003 (CheapEdition). 2. N.H.E. Weste a n d D.M. Harris, "*MOS VLSI d e s i g n : A Circuitsand Systems Perspective*", 4th Edition, Pearson Education India,2011
REFERENCE BOOKS	1. Kang, Sung-Mo, and Yusuf Leblebici. "*CMOS Digital IntegratedCircuits*", Tata McGraw-Hill Education, 2003.

Course Outcomes:

Upon completion of the course, the students will demonstrate the ability to:

CO1	Extract the MOS switchingparameters.
CO2	Carryout efficient design of combinationalcircuits.
CO3	Design the sequentialcircuits.
CO4	Realize logic circuits with different designstyles.
CO5	Demonstrate an understanding of working principle of operation of different typesof memory.

Course Articulation Matrix

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	**3**	**2**	**3**	**3**	**2**	**1**
CO2	**3**	**2**	**3**	**3**	**2**	**1**
CO3	**3**	**2**	**3**	**3**	**2**	**1**
CO4	**3**	**2**	**3**	**3**	**2**	**1**
CO5	**3**	**2**	**3**	**3**	**2**	**1**

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) -: No Correlation

Program Articulation Matrix row for this Course

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
Course	**3**	**2**	**3**	**3**	**2**	**1**

ELECTRONIC DESIGN AUTOMATION

SYLLABUS

Module-I (8 hours)

Introduction: Overview of Electronic Design Automation, Logic Design Automation, Test Automation, Physical Design Automation.

Module-II (8hours)

Design for Testability: Introduction, Testability Analysis, Scan Design, Logic Built-In Self-Test, Test Compression.

Module-III (8 hours)

Fundamentals of Algorithms: Introduction, Computational Complexity, Asymptotic Notations, Complexity Classes, Graph Algorithms, Heuristic Algorithms, Mathematical Programming.

Module-IV (8 hours)

Electronic System-Level Design and High-Level Synthesis: Introduction, Fundamentals of High-Level Synthesis, High-Level Synthesis Algorithm Overview, Scheduling, Register Binding, Functional Unit Binding. ***Logic and Circuit Simulation:***Introduction, Logic Simulation Models, Timing Models, Logic Simulation Techniques, Hardware-Accelerated Logic Simulation,Circuit
Simulation Models, Numerical Methods for Transient Analysis.

Module-V (8 hours)

Memory Design:SRAM, DRAM, ROM, Serial Access Memory,Content Addressable Memory, Field Programmable Gate Array.

Recommended Books

TEXT BOOKS	1.Rabey J.M, A. Chandrakasan, and B.Nicolic, "*Digital Integrated Circuits: A design Perspective*", Second Edition, Pearson/PH, 2003 (CheapEdition). 2. N.H.E. Weste a n d D.M. Harris, "*MOS VLSI d e s i g n : A Circuitsand Systems Perspective*", 4th Edition, Pearson Education India,2011
REFERENCE BOOKS	1. Kang, Sung-Mo, and Yusuf Leblebici. "*CMOS Digital IntegratedCircuits*", Tata McGraw-Hill Education, 2003.

Course Outcomes:

Upon completion of the course, the students will demonstrate the ability to:

CO1	Extract the MOS switchingparameters.
CO2	Carryout efficient design of combinationalcircuits.
CO3	Design the sequentialcircuits.
CO4	Realize logic circuits with different designstyles.

CO5	Demonstrate an understanding of working principle of operation of different typesof memory.

Course Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**3**	**2**	**3**	**3**	**2**	**1**
CO2	**3**	**2**	**3**	**3**	**2**	**1**
CO3	**3**	**2**	**3**	**3**	**2**	**1**
CO4	**3**	**2**	**3**	**3**	**2**	**1**
CO5	**3**	**2**	**3**	**3**	**2**	**1**

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) -: No Correlation

Program Articulation Matrix row for this Course

	PO1	PO2	PO3	PO4	PO5	PO6
Course	**3**	**2**	**3**	**3**	**2**	**1**

VLSI ALGORITHMS

SYLLABUS

Module-I (8 hours)

VLSI Automation Algorithms: General Graph Theory and Basic VLSI Algorithms. ***Partitioning***: Problem Formulation, Classification of Partitioning Algorithms, Group Migration Algorithms, Simulated Annealing & Evolution, Other Partitioning Algorithms.

Module-II (8hours)

Placement, Floor Planning & Pin Assignment: Problem Formulation, Simulation Base Placement Algorithms, Other Placement Algorithms, Constraint-Based Floor Planning, Floor Planning Algorithms for Mixed Block & Cell Design. General & Channel Pin Assignment.

Module-III (8 hours)

Global Routing: Problem Formulation, Classification of Global Routing Algorithms, Maze Routing Algorithm, Line Probe Algorithm, Steiner Tree Based Algorithms, ILP Based Approaches. ***Detailed Routing***: Problem Formulation, Classification of Routing Algorithms, Single Layer Routing Algorithms, Two-Layer Channel Routing Algorithms, Three-Layer Channel Routing Algorithms, And Switchbox Routing Algorithms.

Module-IV (8 hours)

Over the Cell Routing & Via Minimization: Two Layers Over the Cell Routers Constrained & Unconstrained Via Minimization.

Module-V (8 hours)

Compaction: Problem Formulation, One-Dimensional Compaction, Two Dimensions-Based Compaction, Hierarchical Compaction.

Recommended Books

TEXT BOOKS	1. Naveed Shervani, "*Algorithms for VLSI Physical Design Automation*", Academic Publisher, Edition, 2005.Kluwer 2. ThorstenTheobald,"*AlgorithmandDataStructuresforVLSIDesign*", KAP, 2002.
REFERENCE BOOKS	1. Rolf Drechsheler "*Evolutionary Algorithm For VLSI*", Second Edition,2002. Trimburger," *Introduction to CAD For VLSI*", Kluwer Academic Publisher, 2002.

Course Outcomes:

Upon completion of the course, the students will demonstrate the ability to:

CO1	Formulate floorpartitioning.
CO2	Make Placement, Floor Planning & PinAssignment.

CO3	Implement multilayer routing.
CO4	Carryout over the Cell Routing & ViaMinimization.
CO5	Do perfect compaction.

Course Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**3**	**2**	**3**	**3**	**2**	**1**
CO2	**3**	**2**	**3**	**3**	**2**	**1**
CO3	**3**	**2**	**3**	**3**	**2**	**1**
CO4	**3**	**2**	**3**	**3**	**2**	**1**
CO5	**3**	**2**	**3**	**3**	**2**	**1**

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) -: No Correlation

Program Articulation Matrix row for this Course

	PO1	PO2	PO3	PO4	PO5	PO6
Course	**3**	**2**	**3**	**3**	**2**	**1**

VLSI TECHNOLOGY

SYLLABUS

Module-I (8 hours)

***Crystal Growth, Wafer Preparation, Epitaxy and Oxidation*:** Metallurgical Grade Silicon, Electronic Grade Silicon, Czochralski Crystal Growing, Silicon Shaping, Etching, Polishing, Chemical Cleaning, Gettering Treatment, Vapor Phase Epitaxy, Epitaxial Evaluation, Growth Mechanism.

Module-II (8hours)

Oxidation: Oxidation Growth Mechanism and Kinetic Oxidation, Oxidation Techniques and Systems, Oxide Properties, Oxide Induced Defects, Characterization of Oxide Films, Use of Thermal Oxide and CVD Oxide, Growth and Properties of Dry and Wet Oxide, Dopant Distribution, Oxide Quality. ***Diffusion:*** Introduction, Diffusion Equipment and Process, Diffusion Models, Modification of Flick's Law, Oxidation Effects on Diffusion.

Module-III (8 hours)

Ion Implantation – Range Theory, Equipment's, Ion Implantation Parameter Affecting the Dose and Uniformity, Implant Damage and Annealing, ***Etching***: Wet Chemical Etching, Dry Etching. ***Lithography***: Introduction, Photolithographic Process, Photo Resist, Non-Photo Resist, Light Source and Optical Exposure Systems, Pattern Transferring Techniques and Mask Aligner, Optical Lithography, Electron Lithography, X-Ray Lithography, Ion
Lithography.

Module-IV (8 hours)

Dielectric and Polysilicon Film Deposition: Introduction, Deposition Process, Chemical Vapor

Deposition, Physical Vapor Deposition, Polysilicon, Silicon Dioxide, Silicon Nitride, Plasma Assisted Deposition. ***Metallization*** - Different Types of Metallization, Uses & Desired Properties. ***IC Manufacturing***: Electrical Testing,Packaging,Yield.

Module-V (8 hours)

BJT Fabrication and Realization, Overview of MOS Transistor, ***MOS Transistor Process Flow***: MOS Transistor Fabrication, Device Isolation, CMOS Fabrication, Latch - Up In CMOS, BICMOS Technology.

Recommended Books

TEXT BOOKS	1. Gary S. May, Simon M. Sze, "*Fundamentals of Semiconductor Fabrication*", John WileyInc.,2004 *2.* Stephen Cambell, "*The Science and Engineering ofMicroelectronic Fabrication*", Oxford University Press, 2001.
REFERENCE BOOKS	1. Gauranga Bose, "*IC Fabrication Technology*", McGraw hillEducation 2. J. D. Plummer, M. D. Deal and P. B. Griffin, "*Silicon VLSI Technology Fundamentals*", Practice and Models, Prentice Hall,2000.

Course Outcomes:

Upon completion of the course, the students will demonstrate the ability to:

CO1	understand the Fabrication of ICs and purification of Silicon in differenttechnologies
CO2	understand in depth knowledge about the oxidation and doping technique.
CO3	understand the implantation technique and the annealing in the fabrication technique.
CO4	impart in-depth knowledge about etching and deposition of differentlayers.
CO5	understand the different packaging techniques of VLSIdevices

Course Articulation Matrix

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	**3**	**2**	**3**	**3**	**2**	**1**
CO2	**3**	**2**	**3**	**3**	**2**	**1**
CO3	**3**	**2**	**3**	**3**	**2**	**1**
CO4	**3**	**2**	**3**	**3**	**2**	**1**
CO5	**3**	**2**	**3**	**3**	**2**	**1**

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) -: No Correlation

Program Articulation Matrix row for this Course

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
Course	**3**	**2**	**3**	**3**	**2**	**1**

SEMICONDUCTOR DEVICE MODELLING

SYLLABUS

Module-I (8 hours)

PNJunctionDiodeandSchottkyDiode:DCCurrentVoltageCircuits, Static Model, Large Signal Model, Small Signal Model, Schottky Diode and Its Implementation in SPICE 2, Temperature and Area Effect on The Diode Model Parameters, SPICE3, HSPICE &PSPICE Models.

Module-II (8hours)

BJT: Transistor Conversion and Symbols, Ebers-Moll Static, Large Signal and Small Signal Models, Gummel-Poon Static, Large Signal Models, Temperature and Area Effect on The BJT Parameters, Power BJT Models, SPICE3, HSPICE & PSPICE Models.

Module-III (8 hours)

JFET: Static Model, Large Signal Model, Small Signal Model and Its Implementation in SPICE 2, Temperature and Area Effect on The JFET Model Parameters, SPICE3, HSPICE & PSPICE Models.

Module-IV (8 hours)

Metal Oxide Semiconductor Transistor (MOST): Structure and Operating Regions of the MOST, Level-1 And Level-2 Static Models, Level-1 And Level-2 Large-Signal Models, Comment on The Three Models, The Effect of Series Resistance, Small-Signal Models, The Effect of Temperature on The MOST Model Parameters, BSIM1 & BSIM2 Models, SPICE3, HSPICE & PSPICE Models.

Module-V (8 hours)

Noise and Distortion: Noise, Distortion In MOSEFT, ISFET,THYRISTOR.

Recommended Books

TEXT BOOKS	1. G. Massobrio and P.Antognetti, "*Semiconductor Device Modeling by SPICE"*, Second Edition, McGraw Hill, 1993.
REFERENCE BOOKS	1. N. Dasgupta and A. Dasgupta, "*Semiconductor Device Modeling",* PHIPublication

Course Outcomes:

Upon completion of the course, the students will demonstrate the ability to:

CO1	Model adiode.
CO2	Model aBJT.
CO3	Model aJFET.
CO4	Model aMOSFET.
CO5	Model noise anddistortion.

Course Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**3**	**2**	**3**	**3**	**2**	**1**
CO2	**3**	**2**	**3**	**3**	**2**	**1**
CO3	**3**	**2**	**3**	**3**	**2**	**1**
CO4	**3**	**2**	**3**	**3**	**2**	**1**
CO5	**3**	**2**	**3**	**3**	**2**	**1**

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) -: No Correlation

Program Articulation Matrix row for this Course

	PO1	PO2	PO3	PO4	PO5	PO6
Course	**3**	**2**	**3**	**3**	**2**	**1**

JTFA & MRA

SYLLABUS

Module-I (8 hours)

Introduction: Review of Fourier Transform, Parseval Theorem and Need for Joint Time-Frequency Analysis (JTFA), Concept of Non- Stationary Signals, Short-Time Fourier Transforms (STFT), Uncertainty Principle, And Localization/Isolation in Time and Frequency, Hilbert Spaces, Banach Spaces, And Fundamentalsof Hilbert Transform.

Module-II (8hours)

BasesforTime-FrequencyAnalysis:WaveletBasesandFilterBanks, Tilings Of Wavelet Packet and Local Cosine Bases, Wavelet Transform, Real Wavelets, Analytic Wavelets, Discrete Wavelets, InstantaneousFrequency,QuadraticTime-FrequencyEnergy,Wavelet Frames,DyadicWaveletTransform,ConstructionofHaarAndRoof Scaling Function Using Dilation Equation and Graphical Method.

Module-III (8 hours)

Multiresolution Analysis: Haar Multiresolution Analysis (MRA), MRA Axioms, Spanning Linear Subspaces, Nested Subspaces. Orthogonal Wavelets Bases, Scaling Functions, Conjugate Mirror Filters, Haar 2-Band Filter Banks. Study of Up Samplers and Down Samplers. Conditions for Alias Cancellation and Perfect Reconstruction. Discrete Wavelet Transform and Relationship with FilterBanks.FrequencyAnalysisofHaar2-BandFilterBanks,Scaling and Wavelet Dilation Equations in Time and Frequency Domains, Case Study of Decomposition and Reconstruction of GivenSignal Using Orthogonal Framework of Haar 2 Band Filter Bank.

Module-IV (6 hours)

Wavelets: Daubechies Wavelet Bases, Daubechies Compactly Supported Family of Wavelets, Daubechies Filter Coefficient Calculations, Case Study of Daub-4 Filter Design, Connection Between Haar And Daub-4, Concept of Regularity, Vanishing Moments. Other Classes of Wavelets Like Shannon, Meyer, And Battle-Lamarie

Module-V (10 hours)

Bi-Orthogonal Wavelets and Applications: Construction and Design. Case Studies of Biorthogonal 5/3 Tap Design and Its Use in JPEG 2000. Wavelet Packet Trees, Time-Frequency Localization, Compactly Supported Wavelet Packets, Case Study of WalshWavelet PacketBasesGeneratedUsingHaarConjugateMirrorFilterstillDepth

Level3.LiftingSchemesforGeneratingOrthogonalBasesofSecond- Generation Wavelets. ***JTFA Applications***: Riesz Bases, Scalograms, ***Time-Frequency Distributions***: Fundamental Ideas, ***Applications:*** Speech, Audio, Image and Video Compression; SignalDenoising, Feature Extraction, Inverse Problem.

Recommended Books

TEXT BOOKS	1. 1. S.Mallat,"*AWaveletTourofSignalProcessing*,"2ndEdition,Academic Press,1999. 2. L. Cohen, "*Time-frequency analysis*," 1st Edition, Prentice Hall,1995. 3. G.Strang and T. Q. Nguyen, "*Wavelets and Filter Banks*," 2nd Edition, Wellesley Cambridge Press,1998.
REFERENCE BOOKS	1. Daubechies, "Ten Lectures on Wavelets," SIAM,1992. 2. P. P. Vaidyanathan, "*Multirate Systems and Filter Banks*," Prentice Hall, 1993. 3. M. Vetterli and J. Kovacevic, "*Wavelets and Sub band Coding*",Prentice Hall, 1995

Course Outcomes:

Upon completion of the course, the students will demonstrate the ability to:

CO1	Get a survey on evolution of JTFA from the classicaltransforms
CO2	Realize the role of wavelets as bases of time-frequencyanalysis
CO3	Have an in-depth theoretical & mathematical investigation ofwavelets
CO4	Explore the applications of wavelets andJTFA
CO5	Understand application of wavelets incompression.

Course Articulation Matrix

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	**3**	**2**	**3**	**3**	**2**	**1**
CO2	**3**	**2**	**3**	**3**	**2**	**1**
CO3	**3**	**2**	**3**	**3**	**2**	**1**
CO4	**3**	**2**	**3**	**3**	**2**	**1**
CO5	**3**	**2**	**3**	**3**	**2**	**1**

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) -: No Correlation

Program Articulation Matrix row for this Course

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
Course	**3**	**2**	**3**	**3**	**2**	**1**

VLSI DESIGN LABORATORY-I

No.	CONTENTS
1	Design and Simulation of Current Mirror Circuits
2	Design and Simulation of Reference Circuits
3	Design and Simulation of Amplifiers
4	Design and Simulation of CMOS OP-Amp
5	Design and Simulation of Comparators

Course Outcomes:

Upon completion of the course, the students will demonstrate the ability to:

CO1	Design CMOS logic circuits.
CO2	Simulate circuits within a CAD tool and compare to designspecifications
CO3	Analyze the results of logic and timingsimulations and to use these simulation results todebug Analog systems.
CO4	Able to perform power consumption analysis of Analog circuits.
CO5	Design, simulate and Extract the layouts of Analog IC blocks using EDA tools.

Course Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**3**	**3**	**3**	**3**	**3**	**3**
CO2	**3**	**3**	**3**	**3**	**3**	**3**
CO3	**3**	**3**	**3**	**3**	**3**	**3**
CO4	**3**	**3**	**3**	**3**	**3**	**3**
CO5	**3**	**3**	**3**	**3**	**3**	**3**

Program Articulation Matrix row for this Course

	PO1	PO2	PO3	PO4	PO5	PO6
Course	**3**	**3**	**3**	**3**	**3**	**3**

VLSI TECHNOLOGY LABORATORY

No.	CONTENTS
1	Study of crystal Growth and Wafer Preparation
2	Study of Epitaxial Growth
3	Study of Oxidation
4	Study of Lithography
5	Study of Etching
6	Study of Deposition
7	Study of Diffusion
8	Study of Ion Implantation
9	Study of Metallization
10	Study of Packaging

Course Outcomes:

Upon completion of the course, the students will demonstrate the ability to:

CO1	Comprehend impact of semiconductor industry on the design and developmentof integrated system.
CO2	Acquaint with clean room technology.
CO3	Understand oxidation methods, aspects of photolithography diffusion, ion implantation anddeposit techniques.
CO4	Specify NMOS and CMOS design rules corresponding to 180nm, 90nm, 45 nm technologies.
CO5	Understand packaging principles.

Course Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**3**	**3**	**3**	**3**	**3**	**3**
CO2	**3**	**3**	**3**	**3**	**3**	**3**
CO3	**3**	**3**	**3**	**3**	**3**	**3**
CO4	**3**	**3**	**3**	**3**	**3**	**3**
CO5	**3**	**3**	**3**	**3**	**3**	**3**

Program Articulation Matrix row for this Course

	PO1	PO2	PO3	PO4	PO5	PO6
Course	**3**	**3**	**3**	**3**	**3**	**3**

SEMESTER – II

VLSI SIGNAL PROCESSING

SYLLABUS

Module-I (6 hours)

Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital Filters, Parallel Processing. ***Pipelining and Parallel Processing for Low Power. Retiming***: Introduction, Definition and Properties, Solving System of Inequalities, Retiming Techniques.

Module-II (6 hours)

Unfolding: Introduction an Algorithms for Unfolding, Properties of Unfolding, Critical Path, Unfolding and Retiming Application of Unfolding.

Module-III (8 hours)

Folding: Introduction to Folding Transformation, Register Minimization Techniques,Register Minimization in Folded Architectures, Folding in Multirate Systems.

Module-IV (10 hours)

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations Containing Delays.

Module-V (10 hours)

Fast Convolution: Introduction, Cook, Toom Algorithm, Winogard Algorithm, Iterated Convolution, Cyclic Convolution, Design of Fast Convolution Algorithm by Inspection.

Recommended Books

TEXT BOOKS	1. Keshab K. Parhi. "*VLSI Digital Signal Processing Systems"*, Wiley-Inter Sciences, 1999
REFERENCE BOOKS	1. Mohammed Ismail, Terri, Fiez, "*Analog VLSI Signal and Information Processing",* McGraw Hill, 1994. 2. Kung. S.Y., H.J. While house T.Kailath, "*VLSI and Modern signal processing"*, Prentice Hall,1985. 3. Jose E. France, YannisTsividls, "*Design of Analog Digital VLSICircuits for Telecommunications and Signal Processing",* Prentice Hall, 1994.

Course Outcomes:

Upon completion of the course, the students will demonstrate the ability to:

CO1	Understand VLSI design methodology for signal processing systems. Be familiar with VLSI algorithms and architectures forDSP.
CO2	Be able to implement basic architectures for DSP using CADtools.
CO3	Design and analysis of FIR digital filters using pipelinedarchitecture
CO4	Design and analysis of FIR digital filters using parallelprocessing.
CO5	Implementing Cook, Toom Algorithm, WinogardAlgorithms.

Course Articulation Matrix

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	**3**	**2**	**3**	**3**	**2**	**1**
CO2	**3**	**2**	**3**	**3**	**2**	**1**
CO3	**3**	**2**	**3**	**3**	**2**	**1**
CO4	**3**	**2**	**3**	**3**	**2**	**1**
CO5	**3**	**2**	**3**	**3**	**2**	**1**

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) -: No Correlation

Program Articulation Matrix row for this Course

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
Course	**3**	**2**	**3**	**3**	**2**	**1**

DIGITAL SIGNAL PROCESSOR ARCHITECTURES

SYLLABUS

Module-I (6 hours)

Introduction: A Digital Signal-Processing System, Analysis and Design Tool for DSP Systems, ***Computational Accuracy in DSP Implementations***: Number Formats for Signals and Coefficients in DSPSystems,DynamicRangeandPrecision,SourcesofErrorinDSP Implementations-A/D Conversion Errors, DSP ComputationalErrors,D/A Conversion Errors.

Module-II (8 hours)

Architecture for Programmable DSP Devices: Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Module, Programmability and Program Execution, Execution Control-HardwareLooping,Interrupts,Stacks,RelativeBranchSupport,Speed Issues, Pipelining-Pipelining and Performance, Pipeline Depth, Interlocking, Branching Effects, Interrupt Effects, PipelineProgramming Models. Features for External Interfacing.

Module-III (8 hours)

Programmable Digital Signal Processors: Commercial Digital Signal-Processing Devices, The Architecture of TMS320C54XX Processors, Data Addressing Modes of TMS320C54XX Processors, Memory Space of TMS320C54XX Processors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, PipelineOperation of TMS320C54XX Processors.

Module-IV (8 hours)

Implementation of DSP Algorithms: -The Q-Notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, An FFT Algorithm for DFT Computation, A Butterfly Computation-Overflow and Scaling, Bit-Reversed Index Generation, An 8-Point FFT Implementation on The TMS320C54XX, Computation of the Signal Spectrum.

Module-V (8 hours)

Interfacing Memory and Peripherals to DSP Processor: -Memory Space Organization, External Bus Interfacing Signals, Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts and I/O, Direct Memory Access (DMA). A Multichannel Buffered Serial Port (MCBSP), MCBSP Programming, A CODEC Interface Circuit,CODEC Programming, A CODEC-DSP Interface Example.

Recommended Books

TEXT BOOKS	1. Singh, A. and Srinivasan, S., "*Programmable DSP Architecture and Applications"*Thomson,2004./Brooks/Cole,apartofCENGAGELearning 2004. 2. Lapsley, P. et.al, "*DSP Processor Fundamentals: Architectures and Features*", John Wiley & Sons1996 3. Sen M. Kuo, Woon-Seng Gan "DigitalSignal Processors-Architecture, Implementations and Applications", Pearson,2005.
REFERENCE BOOKS	1. Bateman, A. and Yates, W. "*Digital Signal Processing Design"*, Computer Science Press,1989. 2. Texas Instrument "*Digital Signal Processing Applications with the TMS320*

	Family", Prentice-Hall,1988. 3. Texas Instruments, "Linear Circuits: *Data Conversion, DSPAnalog Interface, and Video Interface*", 1992

Course Outcomes:

Upon completion of the course, the students will demonstrate the ability to:

CO1	Know the important basic concepts of Digital Signal Processing and the issuesrelated to computational accuracy of algorithms when implemented using Programmable Digital SignalProcessors.
CO2	Architectural features of programmable DSP devices based on the DSP operations these devices are generally required toperform.
CO3	Know the architecture and programming of programmable DSP devices (DSP320C54XXProcessor).
CO4	Implementation of basic DSP algorithms in programmable DSP devices (DSP320C54XXProcessor).
CO5	Interfacing memory and serial and parallel I/O peripherals to programmableDSP devices (DSP320C54XX Processor).

Course Articulation Matrix

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	**3**	**2**	**3**	**3**	**2**	**1**
CO2	**3**	**2**	**3**	**3**	**2**	**1**
CO3	**3**	**2**	**3**	**3**	**2**	**1**
CO4	**3**	**2**	**3**	**3**	**2**	**1**
CO5	**3**	**2**	**3**	**3**	**2**	**1**

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) -: No Correlation

Program Articulation Matrix row for this Course

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
Course	**3**	**2**	**3**	**3**	**2**	**1**

HIGH LEVEL VLSI DESIGN

SYLLABUS

Module-I (6 hours)

Digital System Design Automation: Digital Design Flow,Verilog HDL, RTL Level Design, Elements of Verilog, Component Description, Test Benches. **Verilog Language Concept**: Characterizing Hardware Languages, Module Basics, Verilog Simulation Model, Compiler Directives.

Module-II (8 hours)

Combinational Circuit Design: Module Wires, Gate Level Logic, Hierarchical Structures, Describing Expressions with Assign Statements, Behavioral Combinational Descriptions, Combinational Synthesis

Module-III (8 hours)

Sequential Circuit Design: Sequential Models,Basic Memory Components, Functional Registers, State Machine Coding, Sequential Synthesis.

Module-IV (8 hours)

Advanced Verilog Topics: Timing and Delays, Detailed Modeling-Switch Level Modeling, Strength Modeling.

Module-V (8 hours)

Processor Design and Test: Processor and Memory Model, Processor Model Specification, Design of Datapath, Control Part Design, Example of CPU Design and Test.

Recommended Books

TEXT BOOKS	1. Z. Navabi, "*Verilog Digital System Design*", Second Edition, Tata McGraw Hill, 2008. 2. S.Palnitkar,"VerilogHDL,*AGuidetoDigitalDesignandSynthesis*",Second Edition, Pearson Education, 2003.
REFERENCE BOOKS	1. S. Brown and Z Vranesic, "Fundamentals *of Digital Logic with Verilog Design*", Mc. Graw Hill Publications, Newyork-2002.

Course Outcomes:

Upon completion of the course, the students will demonstrate the ability to:

CO1	Implement the HDL portion of coding forsynthesis.
CO2	Identify the differences between behavioral and structural coding styles efficient design of sequentialcircuits
CO3	Understand the basic principle of circuit design andanalysis.
CO4	Understand the sequential circuit and itssynthesis.
CO5	Understand the RT level design andtest.

Course Articulation Matrix

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	**3**	**2**	**3**	**3**	**2**	**1**
CO2	**3**	**2**	**3**	**3**	**2**	**1**
CO3	**3**	**2**	**3**	**3**	**2**	**1**
CO4	**3**	**2**	**3**	**3**	**2**	**1**
CO5	**3**	**2**	**3**	**3**	**2**	**1**

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) -: No Correlation

Program Articulation Matrix row for this Course

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
Course	**3**	**2**	**3**	**3**	**2**	**1**

RTL Simulation & Synthesis

SYLLABUS

Module-I (8 hours)

Top-Down Approach to Design: Design of FSMs (Synchronous and Asynchronous), Static Timing Analysis, Meta-Stability, Clock Issues, Need and Design Strategies for Multi-Clock Domain Designs

Module-II (8 hours)

Design Entry: Design Entry by Verilog/VHDL/FSM, Verilog AMS.

Module-III (8 hours)

Programmable Logic Devices: Introduction to ASIC Design Flow, FPGA, SOC, Floor Planning, Placement, Clock Tree Synthesis, Routing, Physical Verification, Power Analysis, ESD Protection

Module-IV (8 hours)

DesignforPerformance:LowPowerVLSIDesignTechniques.Design for Testability.

Module-V (8 hours)

IP And Prototyping: IP In Various Forms: RTL Source Code, Encrypted Source Code, Soft IP, Netlist, Physical IP, Use of External Hard IP During Prototyping. Case Studies and Speed Issues.

Recommended Books

TEXT BOOKS	1. Richard S. Sandige, "*Modern Digital Design*", MGH, International Editions. 2. Donald D Givone, "Digital Principles and Design",TMH 3. CharlesRoth,Jr.AndLizyKJohn,"*DigitalSystemDesignUsingVHDL*", Cengage Learning.
REFERENCE BOOKS	1. 1. SamirPalnitkar,"*VerilogHDL,AGuidetoDigitalDesignandSynthesis*", PrenticeHall. 2. Doug Amos, Austin Lesea, Rene Richter, "*FPGA Based Prototyping Methodology Manual*", Xilinx 3. Bob Zeidman, "*Designing with FPGAs & CPLDs*", CMPBooks.

Course Outcomes:

Upon completion of the course, the students will demonstrate the ability to:

CO1	Learn top-down approach todesign.
CO2	Understand design entry by differentHDL
CO3	Learn the ASIC designflow.
CO4	Know the low power VLSI designtechniques.
CO5	Gather knowledge onIP.

Course Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**3**	**2**	**3**	**3**	**2**	**1**
CO2	**3**	**2**	**3**	**3**	**2**	**1**

CO3	**3**	**2**	**3**	**3**	**2**	**1**
CO4	**3**	**2**	**3**	**3**	**2**	**1**
CO5	**3**	**2**	**3**	**3**	**2**	**1**

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) -: No Correlation

Program Articulation Matrix row for this Course

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
Course	**3**	**2**	**3**	**3**	**2**	**1**

CAD OF DIGITAL SYSTEMS

SYLLABUS

Module-I (8 hours)

IntroductiontoVLSIMethodologies:DesignandFabricationofVLSI Devices, Fabrication Process and its Impact on Design.

Module-II (8 hours)

VLSI Design Automation Tools: Data Structures and Basic Algorithms, Graph Theory and Computational Complexity, Tractable and Intractable Problems.

Module-III (8 hours)

General Purpose Methods for Combinational Optimization: Partitioning, Floor Planning and Pin Assignment, Placement,Routing.

Module-IV (8 hours)

Simulation: Logic Synthesis, Verification, High Level Synthesis.

Module-V (8 hours)

MCMS-VHDL: Verilog-Implementation of Simple Circuits Using VHDL

Recommended Books

TEXT BOOKS	1. N.A. Sherwani, "*Algorithms for VLSI Physical Design Automation*".
REFERENCE BOOKS	1. S.H. Gerez, "*Algorithms for VLSI DesignAutomation*".

Course Outcomes:

Upon completion of the course, the students will demonstrate the ability to:

CO1	Know VLSI designmethodologies
CO2	Learn VLSI automationtools.
CO3	Learn about physical design methods ofVLSI
CO4	Understand the synthesis process inVLSI
CO5	Implementation of simple circuits usingHDL

Course Articulation Matrix

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	**3**	**2**	**3**	**3**	**2**	**1**
CO2	**3**	**2**	**3**	**3**	**2**	**1**

CO3	**3**	**2**	**3**	**3**	**2**	**1**
CO4	**3**	**2**	**3**	**3**	**2**	**1**
CO5	**3**	**2**	**3**	**3**	**2**	**1**

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) -: No Correlation

Program Articulation Matrix row for this Course

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
Course	**3**	**2**	**3**	**3**	**2**	**1**

VLSI DESIGN VERIFICATION & TESTING

SYLLABUS

Module-I (8 hours)

Introduction to SOC and System Verilog Language:Introduction to SOC, History and overview of System Verilog, Language construct, Data Types and operators, Loops, flow control, Task and functions, SV arrays – Queues, Coding of a design.

Module-II (8 hours)

Verification basic and concepts: Functional Verification flows and methodologies, Verification - Planning approach - Metrics, Verification methodologies - Simulation- formal - assertion -directed vs constrained random verification and coverage, Hardware-software verification and Emulation

Module-III (8 hours)

Basic System Verilog Test Benches: Interfaces, Clocking Blocks, Program Blocks, Direct Program Interface, Coding interfaces and clocking blocks.

Module-IV (8 hours)

System Verilog OOPs Concept and Randomization: Basic OOPs Concept, System Verilog Classes, Virtual Interfaces, Random Constraint and usage.

Module-V (8 hours)

Threads and inter processor communication: Process and Threads in System Verilog, System Verilog Mailboxes, Synchronization –Event and semaphore, connecting all TB components using Mailboxes, Built Top TB and compile etc.

Recommended Books

TEXT BOOKS	1. Spear, C. (2008). "System *Verilog For Verification: A Guide to Learning the Testbench Language Features",* Springer Science & Business Media. 2. Vijayaraghavan, S., & Ramanathan, M. (2005). "*A Practical Guide for System Verilog Assertions",* Springer Science & Business Media.
REFERENCE BOOKS	*1. System Verilog 3.1a Language Reference Manual.* 2. Bergeron, J., Cerny, E., Hunter, A., & Nightingale, A. (2006). *"Verification Methodology Manual for System Verilog",* Springer Science & Business Media. 3. Bergeron, J. (2007). "*Writing Testbenches Using System Verilog"*. Springer Science & Business Media.

Course Outcomes:

Upon completion of the course, the students will demonstrate the ability to:

CO1	Familiarity of front-end design and verification techniques and create reusable test environments.
CO2	Verify increasingly complex designs more efficiently and effectively.
CO3	Use EDA tools like Cadence, Mentor Graphics
CO4	Acquire knowledge about fault modeling and collapsing
CO5	Learn about various combinational ATPG and sequence pattern generation

Course Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**3**	**2**	**3**	**3**	**2**	**1**
CO2	**3**	**2**	**3**	**3**	**2**	**1**
CO3	**3**	**2**	**3**	**3**	**2**	**1**
CO4	**3**	**2**	**3**	**3**	**2**	**1**
CO5	**3**	**2**	**3**	**3**	**2**	**1**

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) -: No Correlation

Program Articulation Matrix row for this Course

	PO1	PO2	PO3	PO4	PO5	PO6
Course	**3**	**2**	**3**	**3**	**2**	**1**

LOW POWER VLSI DESIGN

SYLLABUS

Module-I (8 hours)

Technology&CircuitDesignLevels:SourcesofPowerDissipationin Digital ICs, Degree of Freedom, Recurring Themes in Low-Power, Emerging Low Power Approaches, Dynamic Dissipation In CMOS, Effects of V_{DD} & V_T on Speed, Constraints on V_T Reduction, Transistor Sizing&OptimalGateOxideThickness,ImpactofTechnologyScaling, Technology Innovations**.**

Module-II (8 hours)

Low Power Circuit Techniques: Power Consumption in Circuits, Flip- Flops & Latches, High Capacitance Nodes, Energy Recovery, Reversible Pipelines, High Performance Approaches.

Module-III (8 hours)

Low Power Clock Distribution: Power Dissipation in Clock Distribution, Single Driver Versus Distributed Buffers, Buffers & Device Sizing Under Process Variations, Zero Skew Vs. Tolerable Skew, Chip & Package Co-Design of Clock Network.

Module-IV (8 hours)

Logic Synthesis for Low Power Estimation Techniques: Power Minimization Techniques, Low Power Arithmetic Components- Circuit Design Styles, Adders, Multipliers.

Module-V (8 hours)

Low Power Memory Design: Sources & Reduction of Power Dissipation in Memory Subsystem,

Sources of Power Dissipation In DRAM & RAM, Low Power DRAM Circuits, Low Power SRAM Circuits. ***Low Power Microprocessor Design*:** System Power Management Support, Architectural Trade-Offs for Power, Choosing the Supply Voltage, Low-Power Clocking, Implementation Problem for Low Power, Comparison of Microprocessors for Power & Performance.

Recommended Books

TEXT BOOKS	1. P. Rashinkar, Paterson and L. Singh, "*Low Power Design Methodologies*", Kluwer Academic,2002 2. KaushikRoy,SharatPrasad,"*LowPowerCMOSVLSICircuitDesign*",John Wiley sonsInc.,2000. 3. Gary Yeap, "*Practical Low Power Digital VLSI Design*", Kluwer,1998.
REFERENCE BOOKS	1. Rabaey, Pedram, *Low power design methodologies,* Kluwer Academic,1997 2. W.NebelandJ.Mermet,*LowPowerDesigninDeepSub-micronElectronics,* 3. Kluwer Academic Publishers, 1997 4. B.Kulo and J.H Lou, "*Low voltage CMOS VLSI Circuits*", Wiley,1999. 5. A.P.Chandrasekaran and R.W.Broadersen, "*Low Power Digital CMOS Design*",Kluwer,1995

Course Outcomes:

Upon completion of the course, the students will demonstrate the ability to:

CO1	Identify the sources of power dissipation in digital IC systems & understandthe impact of power on system performance and reliability
CO2	Understand various techniques for low power circuitdesign
CO3	Know clock distribution for low powercircuits
CO4	Learn Power Minimization Techniques of Logic Synthesis for LowPower Estimation Techniques
CO5	How to design Low power memory and Microprocessorsystems

Course Articulation Matrix

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	**3**	**2**	**3**	**3**	**2**	**1**
CO2	**3**	**2**	**3**	**3**	**2**	**1**
CO3	**3**	**2**	**3**	**3**	**2**	**1**
CO4	**3**	**2**	**3**	**3**	**2**	**1**
CO5	**3**	**2**	**3**	**3**	**2**	**1**

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) -: No Correlation

Program Articulation Matrix row for this Course

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
Course	**3**	**2**	**3**	**3**	**2**	**1**

DESIGN WITH ASICS

SYLLABUS

Module-I (8 hours)

Types of ASICs: ASIC Design Flow. Programmable ASICs. Anti-Fuse,SRAM,EPROM,EEPROMBasedASICs.ProgrammableASIC Logic Cells and I/O Cells. Programmable Interconnects. AnOverview of Advanced FPGAs and Programmable SOCs: Architecture and ConfigurationofSpartanandVirtexFPGAs.ApexandCyclone FPGAs. Virtex PRO Kits and Nios Kits. OMAP**.**

Module-II (8 hours)

ASIC Physical Design Issues: System Partitioning, Interconnect Delay Models and Measurement of Delay. ASIC Floor Planning, Placement and Routing.

Module-III (8 hours)

Design Issues in SOC: Design Methodologies. Processes and Flows. Embedded Software Development for SOC. Techniques for SOC Testing. Configurable SOC. Hardware/Software Co-design. High Performance Algorithms for ASICs/ SOCs.

Module-IV (8 hours)

SOC Case Studies: DAA and Computation of FFT and DCT. High Performance Filters Using Delta-Sigma Modulators.

Module-V (8 hours)

SOC Case Studies: Digital Camera, Bluetooth Radio/Modem, SDRAM and USB Controllers.

Recommended Books

TEXT BOOKS	1. M.J.S. Smith, *"Application Specific Integrated Circuits",* Pearson, 2003
REFERENCE BOOKS	1. K.K. Parhi, *"VLSI Digital Signal Processing Systems",* John-Wiley, 1999

Course Outcomes:

Upon completion of the course, the students will demonstrate the ability to:

CO1	Learn different ASIC andFPGAs.
CO2	Have knowledge about design issues ofASIC.
CO3	Learn about SOC.
CO4	Compute FFT and DCT.
CO5	Familiar with SOCapplications.

Course Articulation Matrix

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	**3**	**2**	**3**	**3**	**2**	**1**
CO2	**3**	**2**	**3**	**3**	**2**	**1**
CO3	**3**	**2**	**3**	**3**	**2**	**1**
CO4	**3**	**2**	**3**	**3**	**2**	**1**
CO5	**3**	**2**	**3**	**3**	**2**	**1**

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) -: No Correlation

Program Articulation Matrix row for this Course

	PO1	PO2	PO3	PO4	PO5	PO6
Course	**3**	**2**	**3**	**3**	**2**	**1**

VLSI DESIGN LABORATORY-II

No.	CONTENTS
1	Design, Simulation and FPGA Implementation of Arithmetic Circuits.
2	Design, Simulation and FPGA Implementation of Encoder and Decoder Circuit.
3	Design, Simulation and FPGA Implementation of Counters.
4	Design, Simulation and FPGA Implementation of a Simple Microprocessor Data Path.
5	Design, Simulation and FPGA Implementation of a Simple Microprocessor Control Path.
6	Design, Simulation and FPGA Implementation of Memory.

Course Outcomes:

Upon completion of the course, the students will demonstrate the ability to:

CO1	Learn Verilog Language.
CO2	Design combinational logic circuits using Verilog HDL.
CO3	Design Sequential logic circuits using Verilog HDL.
CO4	Implement memories, multipliers, ALU using FPGAs.
CO5	Synthesize Verilog code for special purpose processor using FPGAs.

Course Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**3**	**2**	**3**	**3**	**2**	**1**
CO2	**3**	**2**	**3**	**3**	**2**	**1**
CO3	**3**	**2**	**3**	**3**	**2**	**1**
CO4	**3**	**2**	**3**	**3**	**2**	**1**
CO5	**3**	**2**	**3**	**3**	**2**	**1**

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) -: No Correlation

Program Articulation Matrix row for this Course

	PO1	PO2	PO3	PO4	PO5	PO6
Course	**3**	**2**	**3**	**3**	**2**	**1**

VLSI SIGNAL PROCESSING LABORATORY

No.	CONTENTS
1	Decomposition using Multi Resolution Techniques.
2	Wavelet Coding Techniques
3	Spectral Estimation Using Parametric Method
4	Higher Order Statistics of a Signal
5	PCA/ICA Analysis

Course Outcomes:

Upon completion of the course, the students will demonstrate the ability to:

CO1	Analyze discrete-time signals and systems in various domains.
CO2	Architect programmable DSP devices optimizing the performance.
CO3	Translate effective algorithm design to integrated circuit implementations.
CO4	Learn higher order statistics of signals.
CO5	Analyze various Image Processing algorithms.

Course Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**3**	**2**	**3**	**3**	**2**	**1**
CO2	**3**	**2**	**3**	**3**	**2**	**1**
CO3	**3**	**2**	**3**	**3**	**2**	**1**
CO4	**3**	**2**	**3**	**3**	**2**	**1**
CO5	**3**	**2**	**3**	**3**	**2**	**1**

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) -: No Correlation

Program Articulation Matrix row for this Course

	PO1	PO2	PO3	PO4	PO5	PO6
Course	**3**	**2**	**3**	**3**	**2**	**1**

RFIC

SYLLABUS

Module-I (8 hours)

Introduction: Basic Concepts in RF Design, Passive RLC Networks, Passive IC Components and Their Characteristics**.**

Module-II (8 hours)

Voltage References & Biasing: Supply Independent Biasing, Bandgap Voltage Reference, Constant-g_m biasing. **Feedback Systems**: De-sensitivity, Stability, Errors, Compensation. **Noise**: Thermal noise, Shot Noise, Popcorn Noise, Flicker Noise in devices and circuits.

Module-III (8 hours)

High Frequency Amplifier Design: Zeros as Bandwidth Enhancers, Shunt-Series Amplifiers, Tuned Amplifiers, Cascaded Amplifiers. **LNA design**: LNA Topologies (Power Match and Noise Match), Linearity and Large signal Performance. **RF Power Amplifier**: Class A, Class B, Class C, Class AB Power Amplifiers and their Characteristics.

Module-IV (8 hours)

Oscillators: Tuned oscillators, Negative Resistance Oscillators, Phase Noise. **PLL**: Phase Detectors, Loop Filters, Synthesizers. **Mixers:** Mixer Fundamentals, Non-Linear Systems as Linear Mixers, Mixer Types.

Module-V (8 hours)

Architectures: Transceiver Architecture, Design Examples.

Recommended Books

TEXT BOOKS	1. T. H. Lee, "*The Design of CMOS RF Integrated Circuits*", Cambridge University Press. 2. B. Razavi, "*RF Microelectronics*", Pearson Education.
REFERENCE BOOKS	1. 1 B. Razavi, "*Design of Analog CMOS Integrated Circuits*", Tata Mc Graw Hill, 2002. 2. SorinVoinigescu, "*High Frequency Integrated Circuits*", Cambridge University Press**.** 3. Reinhold Ludwig, Gene Bogdanov, "*RF Circuit Design Theory and Applications*", Pearson Education

Course Outcomes:

Upon completion of the course, the students will demonstrate the ability to:

CO1	Be conversant with RF design concepts, passive on-chip elements
CO2	Understand biasing, feedback and noise
CO3	Design a RF amplifier, Power amplifier, LNA
CO4	Be proficient with frequency conversion and signal generation
CO5	Present the different transceiver architecture.

Course Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	3	3	1	2
CO2	2	---	2	3	2	2
CO3	3	2	3	2	---	1
CO4	3	2	2	2	---	1
CO5	2	1	3	3	2	1

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) ---: No Correlation

Programme Articulation Matrix row for this Course

	PO1	PO2	PO3	PO4	PO5	PO6
Course	3	1	3	3	1	1

FPGA BASED DSP DESIGN

SYLLABUS

Module-I (8 hours)

Multirate Signal Processing: Decimation and Interpolation, Spectrum of Decimated and Interpolated Signals, Polyphase Decomposition of FIR Filters and Its Applications to Multidate DSP. Sampling Rate Converters, Sub-Band Encoder. Filter Banks-Uniform Filter Bank.Direct and DFT Approaches.

Module-II (8 hours)

IntroductiontoADSLModem:DiscreteMultitoneModulationandIts Realization Using DFT. QMF. Short Time Fourier Transform Computation of DWT Using Filter Banks. Implementation and Verification on FPGAs. DDFS- ROM LUT Approach. Spurious SignalsJitter.

Module-III (8 hours)

Software Radio: Block Diagram of A Software Radio. Digital Down Converters and Demodulators. CORDIC Architectures. Universal Modulator and Demodulator Using CORDIC. Computation of Special Functions Using CORDIC. Vector and Rotation Mode Of CORDIC.Implementation and Verification on FPGAs.

Module-IV (8 hours)

Incoherent Demodulation: - Digital Approach for I And Q Generation, Special Sampling Schemes. CIC Filters. Residue Number System and High-Speed Filters Using RNS. Down Conversion Using Discrete Hilbert Transform. Under Sampling
Receivers, Coherent Demodulation Schemes.

Module-V (8 hours)

Speech Coding: Speech Apparatus. Models of Vocal Tract. Speech Coding Using Linear Prediction. CELP Coder. An Overview of Waveform Coding. Vocoders. Vocoder Attributes. Block Diagrams ofEncodersandDecodersofG723.1,G726,G727,G728AndG729

Recommended Books

TEXT BOOKS	1.J. H. Reed, *Software Radio*, Pearson,2002. 2. U. Meyer – Baese, "*Digital Signal Processing with FPGAs"*, Springer,2004
REFERENCE BOOKS	1. Tsui, "*Digital Techniques for Wideband receivers"*, Artech House,2001. 2. S. K. Mitra, "*Digital Signal Processing"*, McGraw Hill,1998 4.

Course Outcomes:

Upon completion of the course, the students will demonstrate the ability to:

CO1	Learn Multirateprocessing
CO2	Design themodem
CO3	Learn CORDICarchitecture
CO4	Design high speed filters using redundant numbersystem
CO5	Understand the basics of speech coding

Course Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**3**	**2**	**3**	**3**	**2**	**1**
CO2	**3**	**2**	**3**	**3**	**2**	**1**
CO3	**3**	**2**	**3**	**3**	**2**	**1**
CO4	**3**	**2**	**3**	**3**	**2**	**1**
CO5	**3**	**2**	**3**	**3**	**2**	**1**

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) -: No Correlation

Program Articulation Matrix row for this Course

	PO1	PO2	PO3	PO4	PO5	PO6
Course	**3**	**2**	**3**	**3**	**2**	**1**

PHYSICAL DESIGN AUTOMATION

SYLLABUS

Module-I (8 hours)

Preliminaries: Introduction to Design Methodologies, Design Automation Tools, Algorithmic Graph Theory, Computational Complexity, Tractable and Intractable Problems. ***General Purpose Methods for Combinational Optimization***: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu Search, Genetic Algorithms.

Module-II (8 hours)

ModelingandSimulation:Gate Level Modeling and Simulation, Switch Level Modelingand Simulation, Layout Compaction, Placement, Floor Planning and Routing Problems,ConceptsandAlgorithms.

Module-III (8 hours)

Logic Synthesis and Verification: Basic Issues and Terminology, Binary-Decision Diagrams, Two-Level Logic Synthesis. ***High-Level Synthesis***: Hardware Models, Internal Representation of The Input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some Aspects of Assignment Problem,

High-Level Transformations.

Module-IV (8 hours)

Physical Design Automation of FPGAs: FPGA Technologies, Physical Design Cycle for FPGAs, Partitioning and Routing for Segmented and Staggered Models. ***Physical Design Automation of MCMs***: MCM Technologies, MCM Physical Design Cycle, Partitioning,.

Module-V (8 hours)

Placement : Chip Array Based and Full Custom Approaches,Routing– Maze Routing, Multiple Stage Routing, Topologic Routing, Integrated Pin –Distribution and Routing, Routing andProgrammable MCMs.

Recommended Books

TEXT BOOKS	1. Naveed Shewani, "*Algorithms for VLSI Physical Design Automation*", Kluwer Academic,1993 2. S.H. Gerez, "*Algorithms for VLSI Design Automation*", John Wiley,1998.
REFERENCE BOOKS	1. S.M. Sait& H. Youssef, "*VLSI Physical Design Automation*", World Scientific,1999. 2. M. Sarrafzadeh, "*Introduction to VLSI Physical Design*", McGraw Hill(IE).

Course Outcomes:

Upon completion of the course, the students will demonstrate the ability to:

CO1	Learn General Purpose Methods for CombinationalOptimization
CO2	Learn techniques of modelling and simulation at different abstractionlevels
CO3	AnalyzephysicaldesignproblemsandEmployappropriateautomationalgorithmsfor Synthesis
CO4	Decompose large mapping problem into pieces, including logic optimization with partitioning, placement androuting
CO5	Know how to place the blocks and how to partition the blocks whilefor designing the layout for IC

Course Articulation Matrix

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	**3**	**2**	**3**	**3**	**2**	**1**
CO2	**3**	**2**	**3**	**3**	**2**	**1**
CO3	**3**	**2**	**3**	**3**	**2**	**1**
CO4	**3**	**2**	**3**	**3**	**2**	**1**
CO5	**3**	**2**	**3**	**3**	**2**	**1**

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) -: No Correlation

Program Articulation Matrix row for this Course

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
Course	**3**	**2**	**3**	**3**	**2**	**1**

PHYSICAL DESIGN AUTOMATION

SYLLABUS

Module-I (8 hours)

Preliminaries: Introduction to Design Methodologies, Design Automation Tools, Algorithmic Graph Theory, Computational Complexity, Tractable and Intractable Problems. ***General Purpose Methods for Combinational Optimization***: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu Search, Genetic Algorithms.

Module-II (8 hours)

ModelingandSimulation:Gate Level Modeling and Simulation, Switch Level Modelingand Simulation, Layout Compaction, Placement, Floor Planning and Routing Problems,ConceptsandAlgorithms.

Module-III (8 hours)

Logic Synthesis and Verification: Basic Issues and Terminology, Binary-Decision Diagrams, Two-Level Logic Synthesis. ***High-Level Synthesis***: Hardware Models, Internal Representation of The Input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some Aspects of Assignment Problem,High-Level Transformations.

Module-IV (8 hours)

Physical Design Automation of FPGAs: FPGA Technologies, Physical Design Cycle for FPGAs, Partitioning and Routing for Segmented and Staggered Models. ***Physical Design Automation of MCMs***: MCM Technologies, MCM Physical Design Cycle, Partitioning,.

Module-V (8 hours)

Placement : Chip Array Based and Full Custom Approaches,Routing– Maze Routing, Multiple Stage Routing, Topologic Routing, Integrated Pin –Distribution and Routing, Routing andProgrammable MCMs.

Recommended Books

TEXT BOOKS	1.Naveed Shewani, "*Algorithms for VLSI Physical Design Automation*", Kluwer Academic,1993 2.S.H. Gerez, "*Algorithms for VLSI Design Automation*", John Wiley,1998.
REFERENCE BOOKS	1. S.M. Sait& H. Youssef, "*VLSI Physical Design Automation*", World Scientific,1999. 2. M. Sarrafzadeh, "*Introduction to VLSI Physical Design*", McGraw Hill(IE).

Course Outcomes:

Upon completion of the course, the students will demonstrate the ability to:

CO1	Learn General Purpose Methods for CombinationalOptimization
CO2	Learn techniques of modelling and simulation at different abstractionlevels
CO3	AnalyzephysicaldesignproblemsandEmployappropriateautomationalgorithmsfor Synthesis
CO4	Decompose large mapping problem into pieces, including logic optimization with partitioning, placement androuting
CO5	Know how to place the blocks and how to partition the blocks whilefor designing the layout for IC

Course Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**3**	**2**	**3**	**3**	**2**	**1**
CO2	**3**	**2**	**3**	**3**	**2**	**1**
CO3	**3**	**2**	**3**	**3**	**2**	**1**
CO4	**3**	**2**	**3**	**3**	**2**	**1**
CO5	**3**	**2**	**3**	**3**	**2**	**1**

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) -: No Correlation

Program Articulation Matrix row for this Course

	PO1	PO2	PO3	PO4	PO5	PO6
Course	**3**	**2**	**3**	**3**	**2**	**1**

SIGNAL PROCESSING

SYLLABUS

Module-I (8 hours)

Overview of DSP: Characterization in Time and Frequency, FFT Algorithms, Digital Filter Design and Structures: Basic FIR/IIR Filter Design & Structures, Design Techniques of Linear Phase FIR Filters, IIR Filters by Impulse Invariance, Bilinear Transformation, FIR/IIR Cascaded Lattice Structures, And Parallel All Pass Realization Of IIR.

Module-II (8 hours)

Multi Rate DSP: Decimators and Interpolators, Sampling Rate Conversion, Multistage Decimator & Interpolator, Poly Phase Filters, QMF, Digital Filter Banks, Applications in Sub-Band Coding. Application of DSP & Multi Rate DSP, Application to Radar, Introduction to Wavelets, Application to Image Processing, Design ofPhase Shifters, DSP In Speech Processing & Other Applications.

Module-III (8 hours)

Linear Prediction & Optimum Linear Filters: Stationary Random Process, Forward-Backward Linear Prediction Filters, Solution of Normal Equations, AR Lattice and ARMA Lattice-Ladder Filters, Wiener Filters for Filtering and Prediction.

Module-IV (8 hours)

Estimation of Spectra from Finite-Duration Observations of Signals. Nonparametric Methods for

Power Spectrum Estimation, Parametric Methods for Power Spectrum Estimation, Minimum Variance Spectral Estimation, Eigen Analysis Algorithms for Spectrum Estimation.

Module-V (8 hours)

Adaptive Filters: Applications, Gradient Adaptive Lattice, Minimum Mean Square Criterion, LMS Algorithm, Recursive Least Square Algorithm.

Recommended Books

TEXT BOOKS	1. J.G. Proakis and D.G. Manolakis, "*Digital Signal Processing*", Third Edition, Prentice Hall. 2. B. Widrow and Stern, "Adaptive Signal Processing".
REFERENCE BOOKS	1. Sanjit K Mitra, "*Digital Signal Processing*", New edition,TMH. 2. Digital Signal Processing, by Salivahanan, New edition,TMH. 3. N. J. Fliege, "*Multirate Digital Signal Processing: Multirate Systems - Filter Banks – Wavelets*", 1st Edition, John Wiley and Sons Ltd,1999. 4. S. Haykin , "*Adaptive Filter Theory*", 4th Edition, Prentice Hall,2001.

Course Outcomes:

Upon completion of the course, the students will demonstrate the ability to:

CO1	Design and analyze the DSP signals andsystems
CO2	Design efficient filters for sampling rate conversion for differentapplications
CO3	Appreciate the significance of normal equations in linear optimum filters and techniques used to solvethem
CO4	Estimate the spectrum of signals from finite-duration observation ofsignals
CO5	Design adaptive filter models for different signal processingapplications

Course Articulation Matrix

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	**3**	**2**	**3**	**3**	**2**	**1**
CO2	**3**	**2**	**3**	**3**	**2**	**1**
CO3	**3**	**2**	**3**	**3**	**2**	**1**
CO4	**3**	**2**	**3**	**3**	**2**	**1**
CO5	**3**	**2**	**3**	**3**	**2**	**1**

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) -: No Correlation

Program Articulation Matrix row for this Course

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
Course	**3**	**2**	**3**	**3**	**2**	**1**

BASICS OF VLSI ENGINEERING

SYLLABUS

Module-I (6 hours)

VLSI Basics. - VLSI – Digital. System: VLSI Design Flow, Y Chart, Design Hierarchy Structural. *VLSI – FPGA Technology*: FPGA – Introduction, Gate Array Design, Standard Cell Based Design, Full Custom Design.

Module-II (8 hours)

VLSI MOS Transistor: Structure of a MOSFET, Working of a MOSFET, MOSFET Current – Voltage Characteristics. ***VLSI – MOS Inverter:***PrincipleofOperation,ResistiveLoadInverter,Inverterwith N type MOSFET Load, Enhancement Load NMOS, DepletionLoad NMOS, CMOS Inverter – Circuit, Operation and Description.

Module-III (6 hours)

VLSI – Combinational MOS Logic Circuits: CMOS Logic Circuits, Complex Logic Circuits, Complex CMOS Logic Gates, ***VLSI – SequentialMOSLogicCircuits***:CMOSLogicCircuits,CMOSLogic Circuits.

Module-IV (10 hours)

VHDL – Introduction: Data Flow Modeling, Behavioral Modeling, StructuralModeling,LogicOperation–ANDGATE,LogicOperation – OR Gate, Logic Operation – NOT Gate, Logic Operation – NAND Gate, Logic Operation – NOR Gate, Logic Operation – XOR Gate, Logic Operation – X-NOR Gate, ***VHDL – Programming for Combinational Circuits:*** VHDL Code for a Half-Adder, VHDL Code for a Full Adder, VHDL Code for a Half-Subtractor, VHDL Code for a Full Subtractor, VHDL Code for a Multiplexer, VHDL Code for a Demultiplexer, VHDL Code for a 8 x 3 Encoder, VHDL Code for a 3 x 8 Decoder, VHDL Code – 4 bit Parallel adder, VHDL Code – 4 bit Parity Checker, VHDL Code – 4 bit Parity Generator, ***VHDL – ProgrammingforSequentialCircuits***;VHDLCodeforanSRLatch, VHDL Code for a D Latch, VHDL Code for an SR Flip Flop, VHDL code for a JK Flip Flop, VHDL Code for a D Flip Flop, VHDL Code foraTFlipFlop,VHDLCodefora4-bitUpCounter,VHDLCode for a 4-bit Down Counter.

Module-V (10 hours)

Verilog – Introduction: Behavioral level, Register−Transfer Level, Gate Level, Lexical Tokens, Gate Level Modelling, Data Types, Operators, Operands, Modules, ***Verilog – Behavioral Modelling & Timing Control***: Procedural Assignments, Delay in Assignment (not for synthesis), Blocking Assignments, Nonblocking (RTL) Assignments, Conditions, Delay Controls, Procedures: Always and Initial Blocks.

Recommended Books

TEXT BOOKS	1. Kang, Sung-Mo, and Yusuf Leblebici. "*CMOS Digital Integrated Circuits*",Tata McGraw-Hill Education, 2003. 2. Volnei A. Pedroni, "*Circuit Design with VHDL*", PHI,2005.
REFERENCE BOOKS	1. N.H.E. Weste a n d D.M. Harris, "*MOS VLSI d e s i g n : A Circuits and Systems Perspective*", 4th Edition, Pearson Education India,2011 2. Z. Navabi, "*Verilog Digital System Design*", Second Edition, Tata McGraw Hill, 2008. 3.Douglas L. Perry, "*VHDL: Programming by Example*", 4th Edition, Tata McGraw Hill, 2004.

Course Outcomes:

Upon completion of the course, the students will demonstrate the ability to:

CO1	Understand basics of VLSI circuits andsystems.
CO2	Understand basic principles of MOS transistor and MOSinverters
CO3	Design combinational as well as sequential logiccircuits.
CO4	Write VHDL programming for logiccircuits.
CO5	Write Verilog programming for logiccircuits

Course Articulation Matrix

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	**3**	**2**	**3**	**3**	**2**	**1**
CO2	**3**	**2**	**3**	**3**	**2**	**1**
CO3	**3**	**2**	**3**	**3**	**2**	**1**
CO4	**3**	**2**	**3**	**3**	**2**	**1**
CO5	**3**	**2**	**3**	**3**	**2**	**1**

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High) -: No Correlation

Program Articulation Matrix row for this Course

	PO1	PO2	PO3	PO4	PO5	PO6
Course	**3**	**2**	**3**	**3**	**2**	**1**