ANALOG ELECTRONICS CIRCUIT

SYLLABUS

Module-I (10 Hours)
DC biasing of BJTs: Load lines, Operating Point, Fixed bias and Voltage-divider bias. DC bias with
voltage feedback, Bias stabilization, Design of bias.
Small Signals Modeling of BJT and their analysis: The r transistor model, Hybrid model, Graphical
determination of h-parameters, Low frequency small signal analysis of CE, CC and CB configurations without
feedback.
Module-II (8 Hours)
DC Biasing of FETs: Fixed bias, Self bias and Voltage divider bias Configuration, Design of bias. Small
Signal Modeling and Analysis of FETs: Small Signal Model, Analysis of JFET C-S and C-D configuration.
System Approach-Effects of R_S and R_L: Two port system, Individual and combined effects of R_S and R_L
on CE, Emitter follower and C-S networks.
Module-III (10 Hours)
BJT and JFET Frequency Response: General frequency considerations, Low frequency analysis of R-C
combination in single stage BJT or FET amplifier- Bode Plot, Lower Cut off frequency for the system, Low
frequency response of BJT and FET amplifiers, Miller Effect Capacitance, High frequency modeling of BJT
and FET, High frequency analysis of BJT and FET amplifiers-Bode plot, Square Wave testing of amplifiers.
Compound Configurations: Cascade, Cascode and Darlington connections, C-MOS Circuits, Current
Source Circuits
Module-IV (12 Hours)
Feedback and Oscillator Circuit: Feedback concept, Type of feedback circuits, Practical feedback
circuit, Analysis of voltage series feedback type amplifier, Effects of negative feedback, Positive feedback,
Barkhausen Criterion of oscillation, Oscillator operation, R-C phase shift oscillator, Wien bridge Oscillator,
Crystal Oscillator, Hartley & Collpit circuits.
Operational Amplifiers: Equivalent Circuit of OP-AMP circuits, Input impedance, OP-AMP
Specifications, DC offset parameters, frequency parameters, Gain-bandwidth, Differential and Common mode
operation, op. amp. Applications: Constant gain multiplier, Voltage summing, Integrator, Differentiator and
Controlled sources.
Power Amplifiers: Definition of A, B and C types, Conversion efficiency, Distortion analysis, Push-pull
configuration.

Text Books:

1. Electronic Devices and Circuit Theory – Robert L.Boylestad and Lowis Nashelsky, 8th Edition Pearson
Publication
2. Integrated Electronics – Millman and Halkias, Mcgraw Hill
3. Microelectronic Circuits – Sedra & Smith, International Student Edition
4. Electronic Devices – Floyd, Pearson Education.

MODULE-I
DC Biasing - BJTs

Objectives

To Understand :

- Concept of Operating point and stability
- Analyzing Various biasing circuits and their comparison with respect to stability

BJT – A Review

- Invented in 1948 by Bardeen, Brattain and Shockley
- Contains three adjoining, alternately doped semiconductor regions: Emitter (E), Base (B), and Collector (C)
- The middle region, base, is very thin
- Emitter is heavily doped compared to collector. So, emitter and collector are not interchangeable.

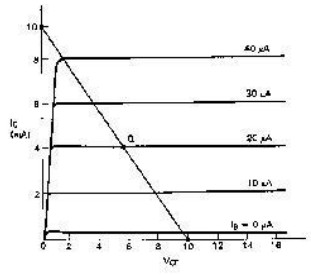
Three operating regions

- **Linear** – **region** operation:
  - Base – emitter junction forward biased
  - Base – collector junction reverse biased
- **Cutoff** – **region** operation:
  - Base – emitter junction reverse biased
  - Base – collector junction reverse biased
- **Saturation** – **region** operation:
  - Base – emitter junction forward biased
  - Base – collector junction forward biased

Three operating regions of BJT

- Cut off: $V_{CE} = V_{CC}$, $I_C \cong 0$
- Active or linear : $V_{CE} \cong V_{CC}/2$, $I_C \cong I_{C\,max}/2$
- Saturation: $V_{CE} \cong 0$, $I_C \cong I_{C\,max}$

Q-Point (Static Operation Point)



- The values of the parameters I_B, I_C and V_{CE} together are termed as 'operating point' or Q (Quiescent) point of the transistor.

Q-Point

- The intersection of the dc bias value of I_B with the dc load line determines the *Q*-point.
- It is desirable to have the *Q*-point centered on the load line. Why?
- When a circuit is designed to have a centered *Q*-point, the amplifier is said to be midpoint biased.
- Midpoint biasing allows optimum ac operation of the amplifier.

Introduction - Biasing

The analysis or design of a transistor amplifier requires knowledge of both the dc and ac response of the system.In fact, the amplifier increases the strength of a weak signal by transferring the energy from the applied DC source to the weak input ac signal

- The analysis or design of any electronic amplifier therefore has two components:
    - The dc portion and
    - The ac portion

During the design stage, the choice of parameters for the required dc levels will affect the ac response.

What is biasing circuit?

- Once the desired dc current and voltage levels have been identified, a network must be constructed that will establish the desired values of I_B, I_C and V_{CE}, Such a network is known as biasing circuit. A biasing network has to preferably make use of one power supply to bias both the junctions of the transistor.

Purpose of the DC biasing circuit

- To turn the device "ON"
- To place it in operation in the region of its characteristic where the device operates most linearly, i.e. to set up the initial dc values of I_B, I_C, and V_{CE}

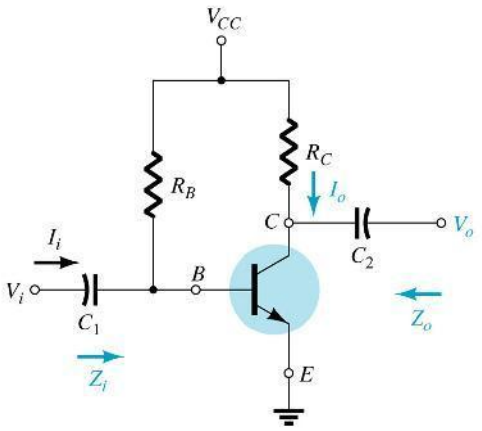
Important basic relationship

- $V_{BE} = 0.7V$
- $I_E = (\beta + 1)\, I_B \cong I_C$
- $I_C = \beta\, I_B$

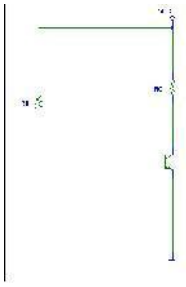
Biasing circuits:

- Fixed – bias circuit
- Emitter bias
- Voltage divider bias
- DC bias with voltage feedback
- Miscellaneous bias

Fixed bias



- The simplest transistor dc bias configuration.
- For dc analysis, open all the capacitance.



DC Analysis

- Applying KVL to the input loop:

$$V_{CC} = I_B R_B + V_{BE}$$

- From the above equation, deriving for IB, we get,

$$I_B = [V_{CC} - V_{BE}] / R_B$$

- The selection of R_B sets the level of base current for the operating point.
- Applying KVL for the output loop:

$$V_{CC} = I_C R_C + V_{CE}$$

- Thus,

$$V_{CE} = V_{CC} - I_C R_C$$

- In circuits where emitter is grounded,

$$V_{CE} = V_E$$
$$V_{BE} = V_B$$

Design and Analysis

- **Design**: Given – I_B, I_C , V_{CE} and V_{CC}, or I_C , V_{CE} and β, design the values of R_B, R_C using the equations obtained by applying KVL to input and output loops.
- **Analysis**: Given the circuit values (V_{CC}, R_B and R_C), determine the values of I_B, I_C , V_{CE} using the equations obtained by applying KVL to input and output loops.

Problem – Analysis

Given the fixed bias circuit with V_{CC} = 12V, R_B = 240 kΩ, R_C = 2.2 kΩ and β = 75. Determine the values of operating point.

Equation for the input loop is:

$$I_B = [V_{CC} - V_{BE}] / R_B \text{ where } V_{BE} = 0.7V,$$

thus substituting the other given values in the equation, we get

$$I_B = 47.08uA$$
$$I_C = \beta I_B = 3.53mA$$
$$V_{CE} = V_{CC} - I_C R_C = 4.23V$$

- When the transistor is biased such that I_B is very high so as to make I_C very high such that $I_C R_C$ drop is almost V_{CC} and V_{CE} is almost 0, the transistor is said to be in saturation.

$$I_C \text{ sat} = V_{CC} / R_C \quad \text{in a fixed bias circuit.}$$

Verification

- Whenever a fixed bias circuit is analyzed, the value of I_{CQ} obtained could be verified with the value of I_{CSat} (= V_{CC} / R_C) to understand whether the transistor is in active region.
- In active region,

$$I_{CQ} = (I_{CSat} /2)$$

Load line analysis

A fixed bias circuit with given values of V_{CC}, R_C and R_B can be analyzed (means, determining the values of I_{BQ}, I_{CQ} and V_{CEQ}) using the concept of load line also. Here the input loop KVL equation is not used for the purpose of analysis, instead, the output characteristics of the transistor used in the given circuit and output loop KVL equation are made use of.

- The method of load line analysis is as below:

1. Consider the equation $V_{CE} = V_{CC} - I_C R_C$ This relates V_{CE} and I_C for the given I_B and R_C

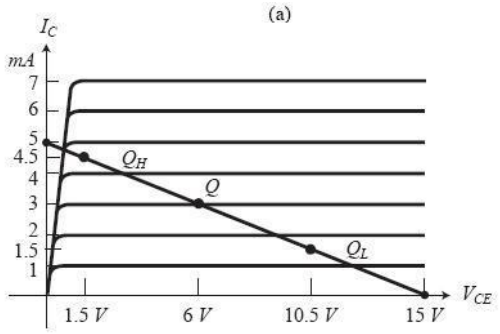
2. Also, we know that, V_{CE} and I_C are related through output characteristics We know that the equation,

$$V_{CE} = V_{CC} - I_C R_C$$

represents a straight line which can be plotted on the output characteristics of the transistor.

Such line drawn as per the above equation is known as load line, the slope of which is decided by the value of R_C (the load).

Load line



- The two extreme points on the load line can be calculated and by joining which the load line can be drawn.
- To find extreme points, first, Ic is made 0 in the equation: $V_{CE} = V_{CC} - I_C R_C$. This gives the coordinates $(V_{CC},0)$ on the x axis of the output characteristics.
- The other extreme point is on the y-axis and can be calculated by making $V_{CE} = 0$ in the equation $V_{CE} = V_{CC} - I_C R_C$ which gives $I_{C(\ max)} = V_{CC} / R_C$ thus giving the coordinates of the point as $(0, V_{CC} / R_C)$.
- The two extreme points so obtained are joined to form the load line.
- The load line intersects the output characteristics at various points corresponding to different I_Bs. The actual operating point is established for the given I_B.

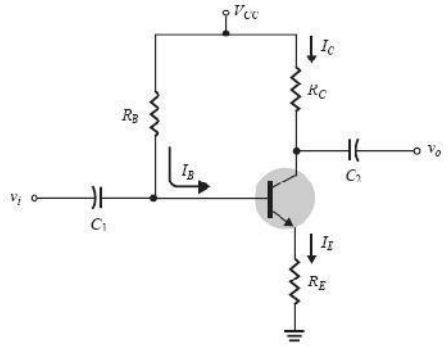
Q point variation

As I_B is varied, the Q point shifts accordingly on the load line either up or down depending on I_B increased or decreased respectively.

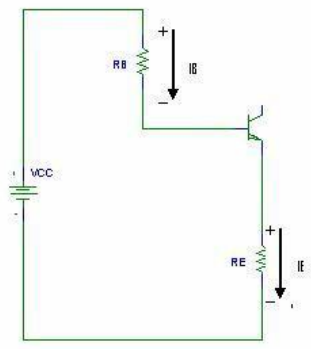
As R_C is varied, the Q point shifts to left or right along the same I_B line since the slope of the line varies. As R_C increases, slope reduces (slope is $-1/R_C$) which results in shift of Q point to the left meaning no variation in I_C and reduction in V_{CE} . Thus if the output characteristics is known, the analysis of the given fixed bias circuit or designing a fixed bias circuit is possible using load line analysis as mentioned above.

Emitter Bias

- It can be shown that, including an emitter resistor in the fixed bias circuit improves the stability of Q point.
- Thus emitter bias is a biasing circuit very similar to fixed bias circuit with an emitter resistor added to it.



Input loop



- Writing KVL around the input loop we get,

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E \quad (1)$$

We know that,

$$I_E = (\beta+1) I_B \quad (2)$$

Substituting this in (1), we get,

$$V_{CC} = I_B R_B + V_{BE} + (\beta+1) I_B R_E$$

$$V_{CC} - V_{BE} = I_B (R_B + (\beta+1) R_E)$$

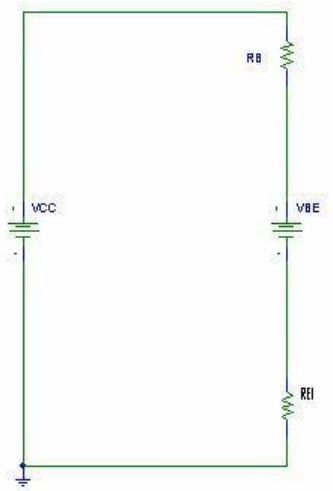
Solving for I_B:

$$I_B = (V_{CC} - V_{BE}) / [(R_B + (\beta+1) R_E)]$$

The expression for I_B in a fixed bias circuit was,

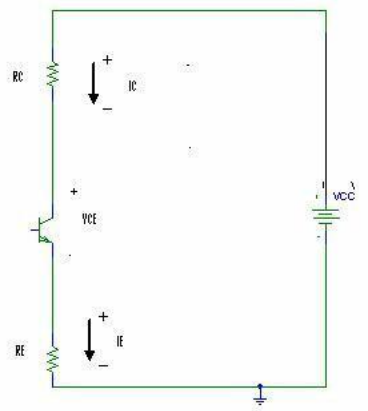
$$I_B = (V_{CC} - V_{BE}) / R_B$$

Equivalent input loop:



- R_{EI} in the above circuit is $(\beta+1)R_E$ which means that, the emitter resistance that is common to both the loops appears as such a high resistance in the input loop.
- Thus $Ri = (\beta+1)R_E$ (more about this when we take up ac analysis)

Output loop



Collector – emitter loop

Applying KVL,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

I_C is almost same as I_E

Thus,

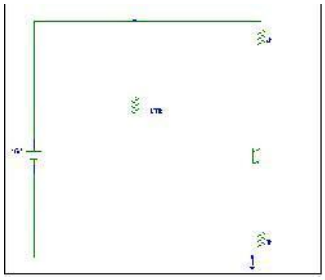
$$V_{CC} = I_C R_C + V_{CE} + I_C R_E$$
$$= I_C (R_C + R_E) + V_{CE}$$
$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Since emitter is not connected directly to ground, it is at a potential V_E, given by,

$$V_E = I_E R_E$$
$$V_C = V_{CE} + V_E \textbf{ OR } V_C = V_{CC} - I_C R_C$$
$$\text{Also, } V_B = V_{CC} - I_B R_B \textbf{ OR } V_B = V_{BE} + V_E$$

Problem:

Analyze the following circuit: given
$\beta = 75$, $V_{CC} = 16V$, $R_B = 430k\Omega$, $R_C = 2k\Omega$ and $R_E = 1k\ \Omega$



Solution:

$I_B = (V_{CC} - V_{BE}) / [(R_B + (\beta+1) R_E)]$

$= (16 - 0.7) / [430k + (76) 1k] =$

$30.24\mu A$ $I_C = (75) (30.24\mu A) = 2.27mA$

$V_{CE} = V_{CC} - I_C (R_C + R_E) = 9.19V$

$V_C = V_{CC} - I_C R_C = 11.46V$

$V_E = V_C - V_{CE} = 2.27V$

$V_B = V_{BE} + V_E = 2.97V$

$V_{BC} = V_B - V_C = 2.97 - 11.46 = - 8.49V$

Improved bias stability

- Addition of emitter resistance makes the dc bias currents and voltages remain closer to their set value even with variation in
  - transistor beta
  - temperature

Stability

In a fixed bias circuit, I_B does not vary with β and therefore whenever there is an increase in β, I_C increases proportionately, and thus V_{CE} reduces making the Q point to drift towards saturation.In an emitter bias circuit, As β increases, I_B reduces, maintaining almost same I_C and V_{CE} thus stabilizing the Q point against β variations.

Saturation current

In saturation V_{CE} is almost 0V, thus

$$V_{CC} = I_C (R_C + R_E)$$

Thus, saturation current

$$I_{C,sat} = V_{CC} / (R_C + R_E)$$

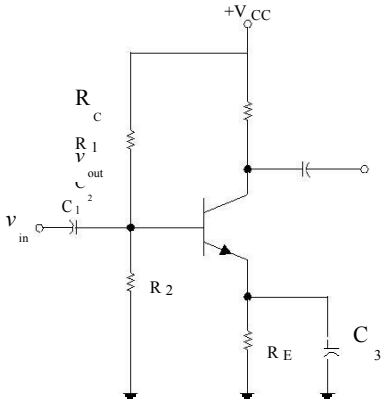
Load line analysis

The two extreme points on the load line of an emitter bias circuit are,

(0, $V_{CC} / [R_C + R_E]$) on the Y axis, and

(V_{CC}, 0) on the X axis.

Voltage divider bias



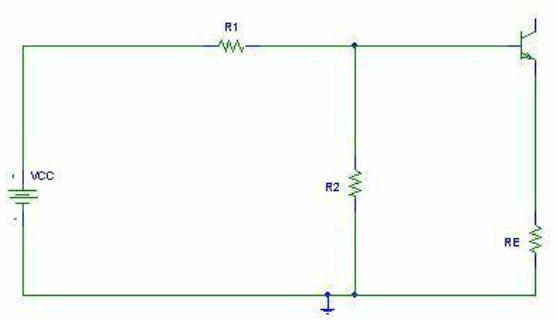
This is the biasing circuit wherein, I_{CQ} and V_{CEQ} are almost independent of β.

The level of I_{BQ} will change with β so as to maintain the values of I_{CQ} and V_{CEQ} almost same, thus maintaining the stability of Q point.

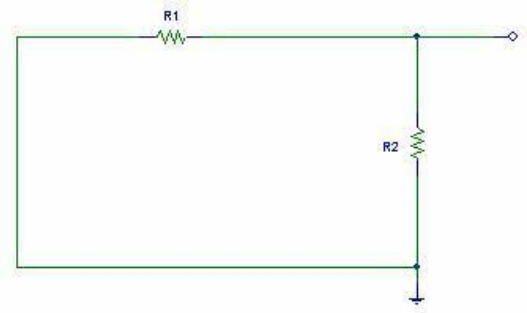
Two methods of analyzing a voltage divider bias circuit are:
Exact method – can be applied to any voltage divider circuit
Approximate method – direct method, saves time and energy, can be applied in most of the circuits.

Exact method

In this method, the Thevenin equivalent network for the network to the left of the base terminal to be found.



To find Rth:

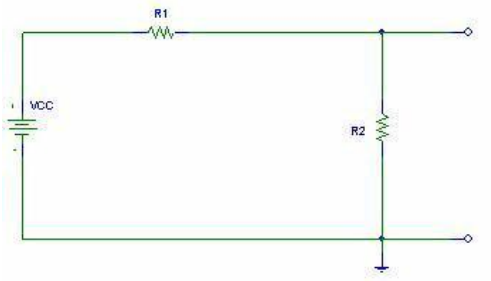


From the above circuit,

$$R_{th} = R1 \,||\, R2$$

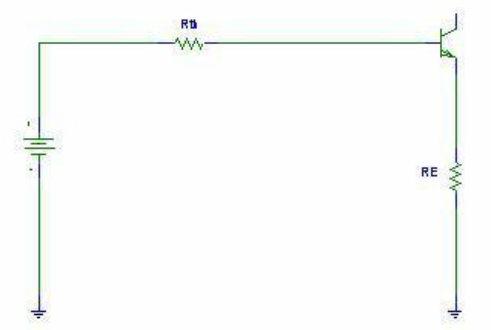
$$= R1\ R2 / (R1 + R2)$$

To find Eth



From the above circuit,

$$E_{th} = V_{R2} = R_2 V_{CC} / (R1 + R2)$$



In the above network, applying KVL

$$(E_{th} - V_{BE}) = I_B [R_{th} +(\beta + 1) R_E]$$

$$I_B = (E_{th} - V_{BE}) / [R_{th} +(\beta + 1) R_E]$$

Analysis of Output loop

KVL to the output loop:

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

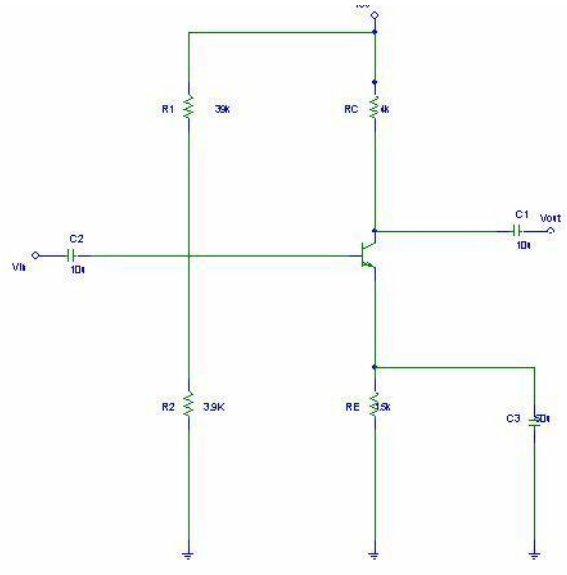
$$I_E \cong I_C$$

Thus, $$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Note that this is similar to emitter bias circuit**.**

Problem

For the circuit given below, find I_C and V_{CE}.
Given the values of R_1, R_2, R_C, R_E and $\beta = 140$ and $V_{CC} = 18V$.
For the purpose of DC analysis, all the capacitors in the amplifier circuit are opened.



Solution

Considering exact analysis:

1. Let us find $R_{th} = R1 \,||\, R2$

$= R1\ R2 / (R1 + R2) = 3.55K$

2. Then find $E_{th} = V_{R2} = R2V_{CC} / (R1 + R2)$

$= 1.64V$

3. Then find IB

$I_B = (Eth - V_{BE}) / [Rth + (\beta + 1) R_E]$

$= 4.37\mu A$

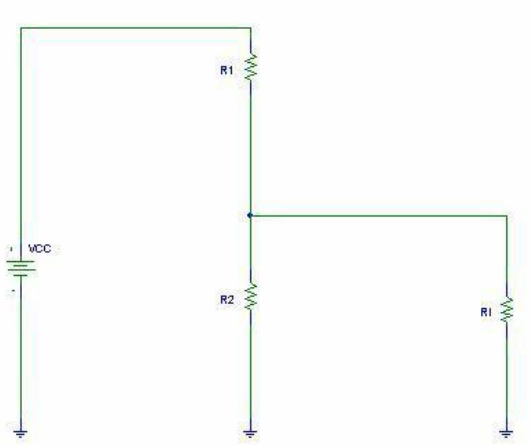
4. Then find $I_C = \beta I_B = 0.612mA$

5. Then find $V_{CE} = V_{CC} - I_C (RC + RE)$
$= 12.63V$

Approximate analysis:

The input section of the voltage divider configuration can be represented by the network shown in the next slide.

Input Network



The emitter resistance R_E is seen as $(\beta+1)R_E$ at the input loop.
If this resistance is much higher compared to R_2, then the current I_B is much smaller than I_2 through R_2.
This means, $Ri >> R2$

OR

$(\beta+1)R_E \geq 10R2$

OR

$\beta R_E \geq 10R2$

This makes I_B to be negligible.
Thus I_1 through R_1 is almost same as the current I_2 through R_2.
Thus R_1 and R_2 can be considered as in series.
Voltage divider can be applied to find the voltage across R_2 (V_B)

$$V_B = V_{CC}R_2 / (R_1 + R_2)$$

Once V_B is determined, V_E is calculated as,

$$V_E = V_B - V_{BE}$$

After finding V_E, I_E is calculated as,

$$I_E = V_E / R_E$$
$$I_E \cong I_C$$
$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Problem

Given: V_{CC} = 18V, R_1 = 39k **Ω**, R_2 = 3.9k **Ω**, R_C = 4k **Ω**, R_E = 1.5k **Ω** and β = 140. Analyse the circuit using approximate technique.
In order to check whether approximate technique can be used, we need to verify the condition,

$$\beta R_E \geq 10R_2$$

Here,

$$\beta R_E = 210\ k\Omega \text{ and } 10R_2 = 39\ k\Omega$$

Thus the condition

$$\beta R_E \geq 10R_2 \text{ satisfied}$$

Solution

- Thus approximate technique can be applied.

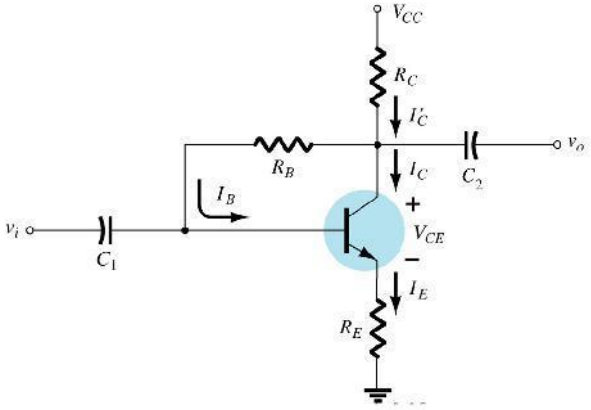
1. Find $V_B = V_{CC}R_2 / (R_1 + R_2) = 1.64V$
2. Find $V_E = V_B – 0.7 = 0.94V$
3. Find $I_E = V_E / R_E = 0.63mA = I_C$
4. Find $V_{CE} = V_{CC} – I_C(R_C + R_E) = 12.55V$

Comparison

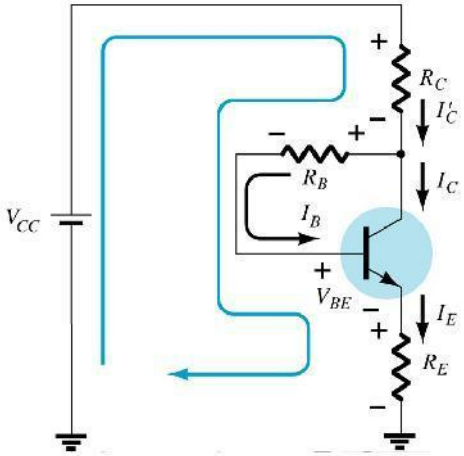
Exact Analysis	**Approximate Analysis**
I_C = 0.612mA	**I_C = 0.63mA**
V_{CE} = 12.63V	**V_{CE} = 12.55V**

Both the methods result in the same values for I_C and V_{CE} since the condition $\beta R_E \geq 10R_2$ is satisfied.
It can be shown that the results due to exact analysis and approximate analysis have more deviation if the above mentioned condition is not satisfied.
For load line analysis of voltage divider network, $I_{c,max} = V_{CC}/ (R_C+R_E)$ when $V_{CE} = 0V$ and $V_{CE\ max} = V_{CC}$ when $I_C = 0$.

DC bias with voltage feedback



Input loop



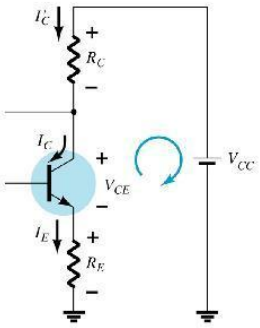
Applying KVL for Input Loop:

$$V_{CC} = I_{C1}R_C + I_BR_B + V_{BE} + I_ER_E$$

Substituting for I_E as $(\beta +1)I_B$ and solving for I_B,

$$I_B = (V_{CC} - V_{BE}) / [R_B + \beta(R_C + R_E)]$$

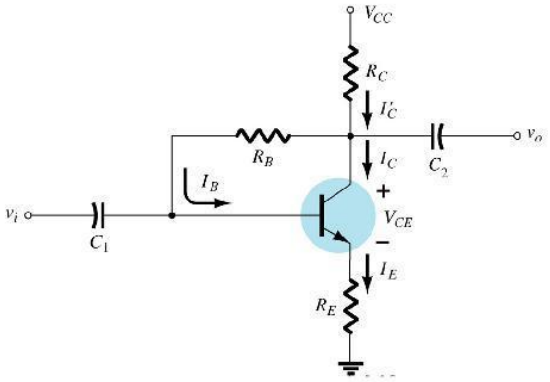
Output loop



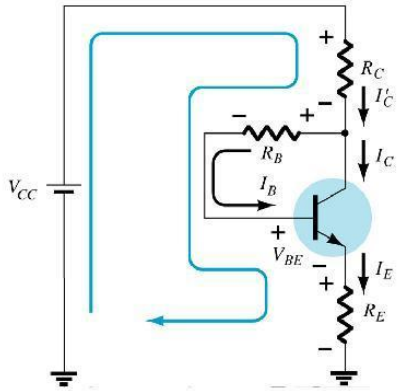
Neglecting the base current, KVL to the output loop results in,

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

DC bias with voltage feedback



Input loop



Applying KVL to input loop:

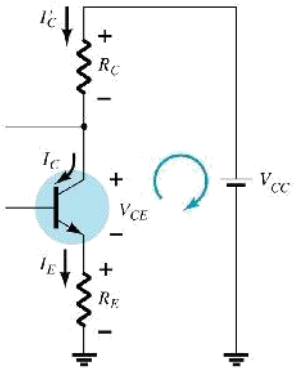
$$V_{CC} = I_C' R_C + I_B R_B + V_{BE} + I_E R_E$$

$I_C' \cong I_C$ and $I_C \cong I_E$

Substituting for I_E as $(\beta + 1) I_B$ [or as βI_B] and solving for

I_B, $I_B = (V_{CC} - V_{BE}) / [R_B + \beta(R_C + R_E)]$

Output loop



Neglecting the base current, and applying KVL to the output loop results in,

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

In this circuit, improved stability is obtained by introducing a feedback path from collector to base.
Sensitivity of Q point to changes in beta or temperature variations is normally less than that encountered for the fixed bias or emitter biased configurations.

Problem:

Given:

V_{CC} = 10V, R_C = 4.7k, R_B = 250Ω and R_E = 1.2k. β = 90.
Analyze the circuit.

$$I_B = (V_{CC} - V_{BE}) / [R_B + \beta(R_C + R_E)]$$

$$= 11.91\mu A$$

$$I_C = (\beta I_B) = 1.07mA$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E) = 3.69V$$

In the above circuit, Analyze the circuit if β = 135 (50% increase).

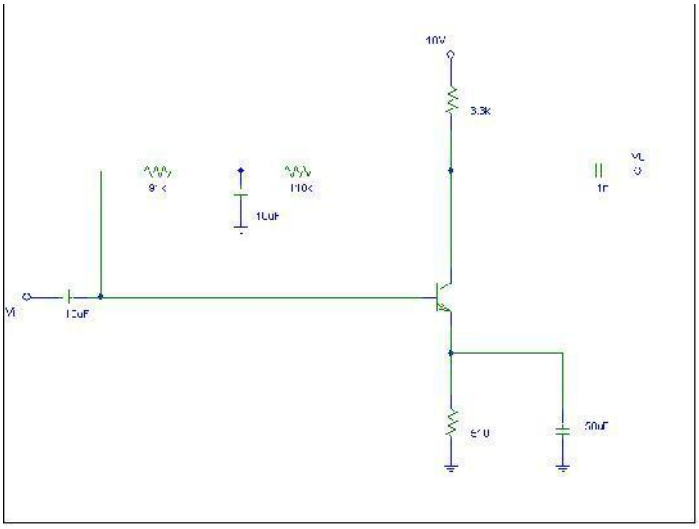
With the same procedure as followed in the previous problem, we get

- I_B = 8.89μA
- I_C = 1.2mA
- V_{CE} = 2.92V

50% increase in β resulted in 12.1% increase in I_C and 20.9% decrease in V_{CEQ}

Problem 2:

Determine the DC level of I_B and V_C for the network shown:



Solution:

Open all the capacitors for DC analysis.

$$R_B = 91\ k\Omega + 110\ k\Omega = 201k$$

$$I_B = (V_{CC} - V_{BE}) / [R_B + \beta(R_C + R_E)]$$

$$= (18 - 0.7) / [201k + 75(3.3+0.51)]$$

$$= 35.5\mu A$$

$$I_C = \beta I_B = 2.66mA$$

$$V_{CE} = V_{CC} - (I_C R_C)$$

$$= 18 - (2.66mA)(3.3k)$$

$$= 9.22V$$

Load line analysis

The two extreme points of the load line $I_{C,max}$ and $V_{CE,\ max}$ are found in the same as a voltage divider circuit.

$I_{C,max} = V_{CC} / (R_C + R_E)$ – Saturation current

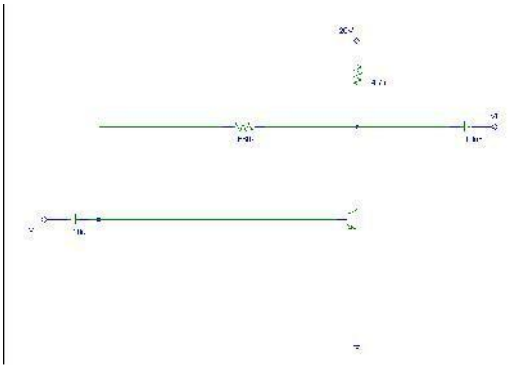
$V_{CE,\ max}$ – Cut off voltage

Miscellaneous bias configurations

There are a number of BJT bias configurations that do not match the basic types of biasing that are discussed till now.

Miscellaneous bias (1)

Analyze the circuit in the next slide. Given $\beta = 120$

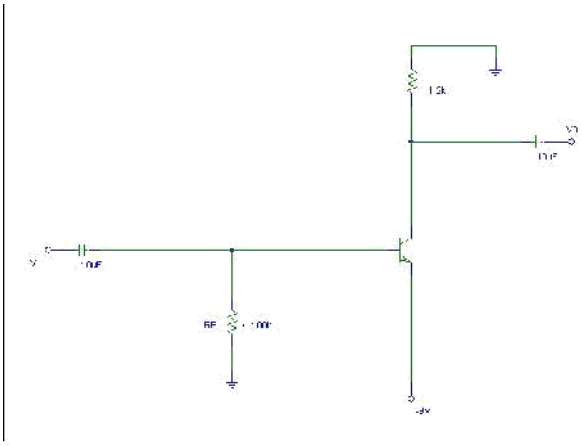


Solution

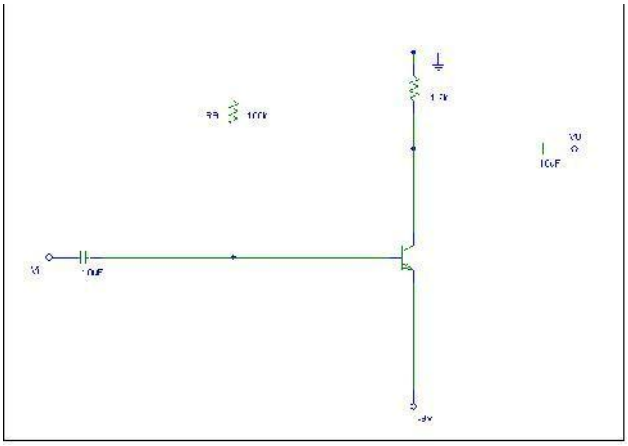
This circuit is same as DC bias with voltage feedback but with no emitter resistor. Thus the expression for I_B is same except for R_E term.

$$I_B = (V_{CC} - V_{BE}) / (R_B + \beta R_C)$$
$$= (20 - 0.7) / [680k + (120)(4.7k)]$$
$$= 15.51\mu A$$
$$I_C = \beta I_B = 1.86mA$$
$$V_{CE} = V_{CC} - I_C R_C = 11.26V = V_{CE}$$
$$V_B = V_{BE} = 0.7V$$
$$V_{BC} = V_B - V_C = 0.7V - 11.26V = - 10.56V$$

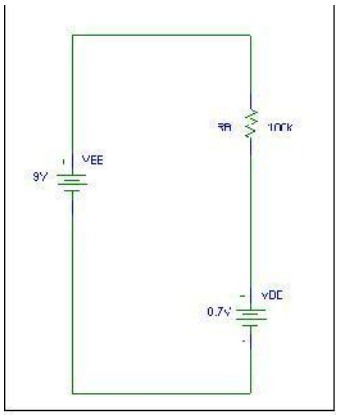
Miscellaneous bias (2)



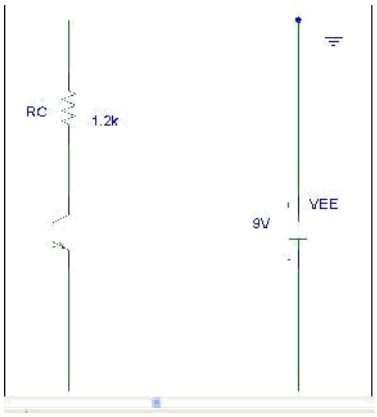
Equivalent circuit



Input loop



Output loop



Solution

The above circuit is fixed bias circuit.

Applying KVL to input loop:

$$V_{EE} = V_{BE} + I_B R_B$$

$$I_B = (V_{EE} - V_{BE}) / R_B = 83\mu A$$

$$I_C = \beta I_B = 3.735mA$$

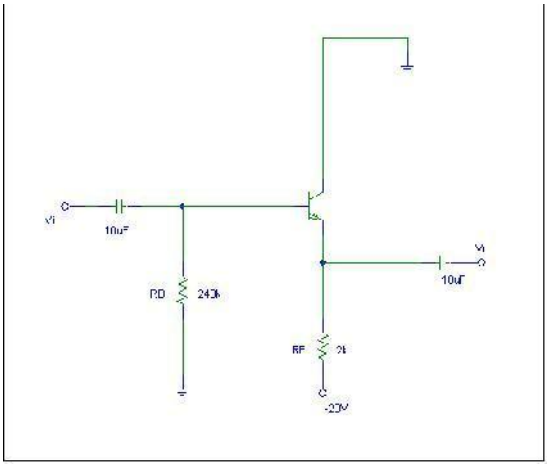
$$V_C = -I_C R_C = - 4.48V$$

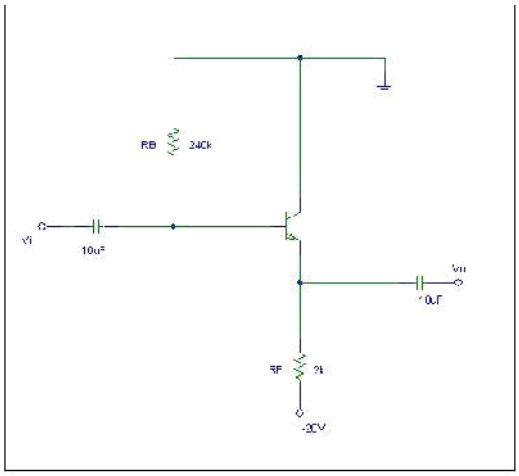
$$V_B = - I_B R_B = - 8.3V$$

Miscellaneous bias (3)

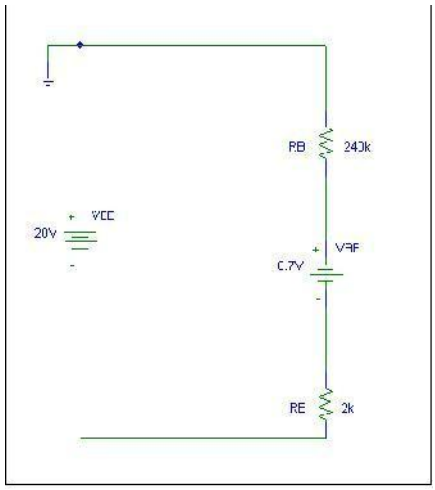
Determine $V_{CE,Q}$ and I_E for the network. Given $\beta = 90$

(Note that the circuit given is common collector mode which can be identified by No resistance connected to the collector output taken at the emitter)





Input loop



Writing KVL to input loop:

$$V_{EE} = I_B R_B + V_{BE} + (\beta+1) I_B R_E$$

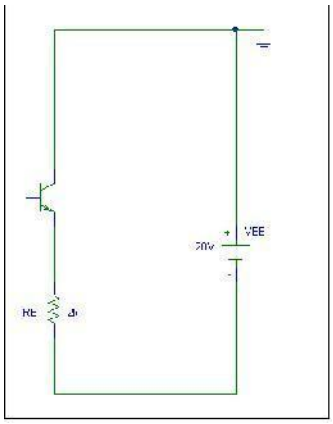
$$I_B = (V_{EE} - V_{BE}) / [R_B + (\beta+1) R_E]$$

$$= (20 - 0.7) / [240K + (91)(2K)]$$

$$= 45.73\mu A$$

$$I_C = \beta I_B = 4.12mA$$

Output loop



Applying KVL to the output loop:

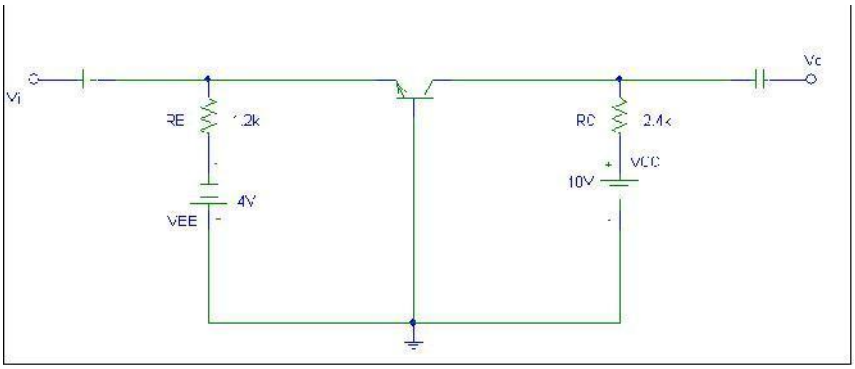
$$V_{EE} = V_{CE} + I_E R_E$$

$I_E = (\beta+1)\, I_B = 4.16\text{mA}$, $V_{EE} = 20\text{V}$

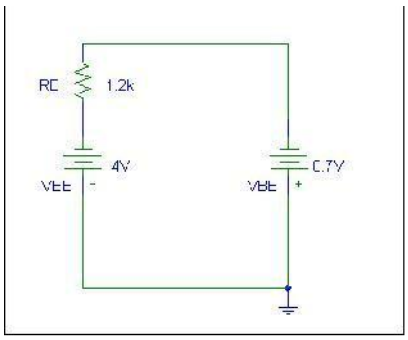
$$V_{CE} = V_{EE} - I_E R_E = 11.68\text{V}$$

Miscellaneous bias (4)

Find V_{CB} and I_B for the Common base configuration given: Given: $\beta = 60$



Input loop



Applying KVL to input loop

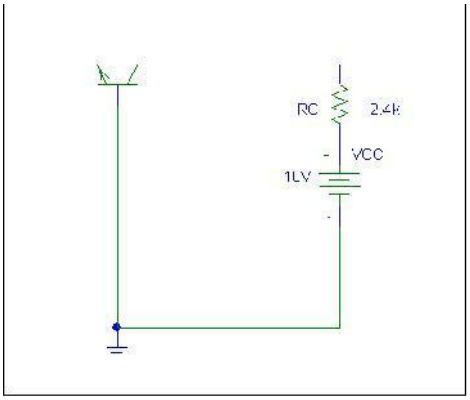
$$I_E = (V_{EE} - V_{BE}) / R_E$$

$$= 2.75mA$$

$$I_E = I_C = 2.75mA$$

$$I_B = I_C / \beta = 45.8\mu A$$

Output loop



Applying KVL to output loop:

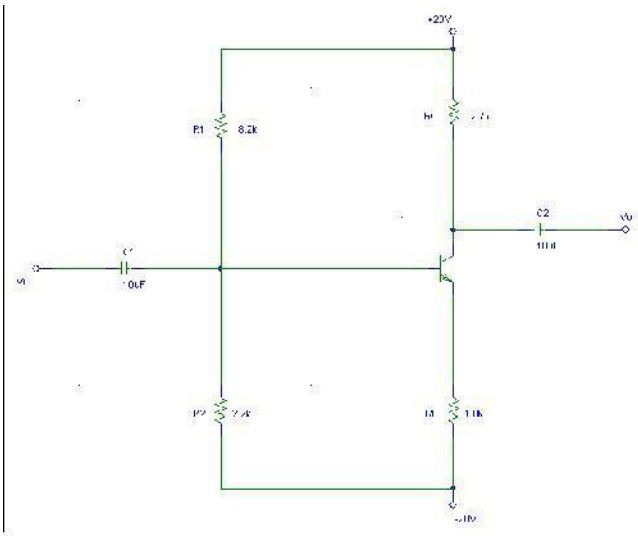
$$V_{CC} = I_C R_C + V_{CB}$$

$V_{CB} = V_{CC} - I_C R_C = 3.4V$

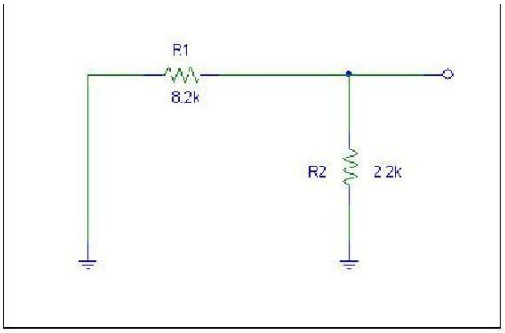
Miscellaneous bias (5)

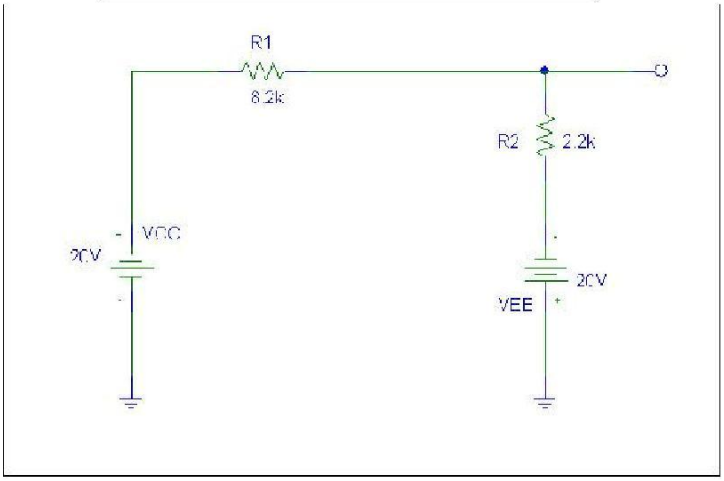
Determine VC and VB for the network given below. Given $\beta = 120$

Note that this is voltage divider circuit with split supply. ($+V_{CC}$ at the collector and $- V_{EE}$ at the emitter)



Thevinin equivalent at the input





R_{th}= (8.2k)(2.2k) / [8.2k+2.2k] = 1.73k

$$I = (V_{CC} + V_{EE}) / [R_1 + R_2]$$

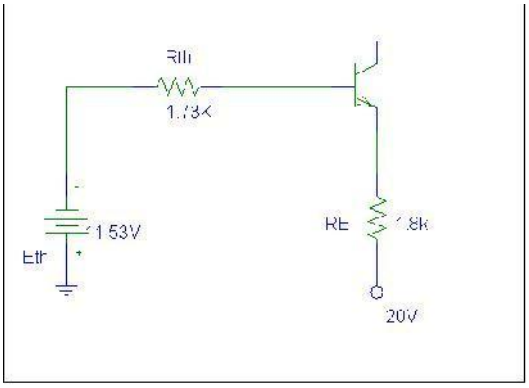
$$= (20 + 20) / (8.2K + 2.2K)$$

$$= 3.85mA$$

$$E_{th} = IR_2 – V_{EE}$$

$$= - 11.53V$$

Equivalent circuit



Applying KVL:

$$V_{EE} - E_{th} - V_{BE} - (\beta +1)I_BR_E - I_BR_{th} = 0$$

$$I_B = (V_{EE} - E_{th} - V_{BE}) / [(\beta +1) R_E + R_{th}]$$

$$= 35.39\mu A$$

$$I_C = \beta I_B = 4.25mA$$

$$V_C = V_{CC} - I_CR_C = 8.53V$$

$$V_B = - E_{th} - I_BR_{th} = - 11.59V$$

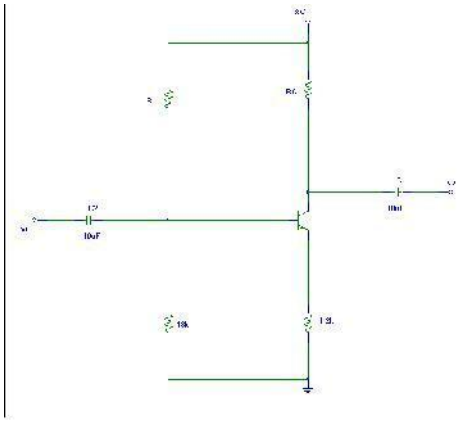
Design Operations:

Designing a circuit requires

- Understanding of the characteristics of the device
- The basic equations for the network
- Understanding of Ohms law, KCL, KVL
- If the transistor and supplies are specified, the design process will simply determine the required resistors for a particular design.
- Once the theoretical values of the resistors are determined, the nearest standard commercial values are normally chosen.
- Operating point needs to be recalculated with the standard values of resistors chosen and generally the deviation expected would be less than or equal to 5%.

Problem:

- Given I_{CQ} = 2mA and V_{CEQ} = 10V. Determine R_1 and R_C for the network shown:



Solution

To find R_1:

1. Find V_B. And to find V_B, find V_E because, $V_B = V_E + V_{BE}$
2. Thus, $V_E = I_E R_E$ and $I_E \cong I_C = 2mA$
   $= (2mA)(1.2k) = 2.4V$
3. $V_B = 2.4 + 0.7 = 3.1V$
4. Also, $V_B = V_{CC} R_2 / (R_1 + R_2)$
   $3.1 = (18)(18k) / R1+18k$
   Thus, $R_1 = 86.52k\Omega$

To find R_C :

Voltage across $R_C = V_{CC} - (V_{CE} + I_E R_E)$
$= 18 - [10 + (2mA)1.2k]$
$= 5.6V$
$R_C = 5.6/2mA$
$= 2.8K\Omega$

Nearest standard values are,
$R_1 = 82k\Omega + 4.7\ k\Omega = 86.7\ k\ \Omega$ where as calculated value is 86.52 k Ω
. $R_C = 2.7k$ in series with $1k = 2.8k$

both would result in a very close value to the design level.

Problem 2

The emitter bias circuit has the following specifications: $I_{CQ} = 1/2I_{sat}$, $I_{sat} = 8mA$, $V_C = 18V$, $V_{CC} = 18V$ and $\beta = 110$. Determine R_C , R_E and R_B.

Solution:

$I_{CQ} = 4mA$

$V_{RC} = (V_{CC} - V_C) = 10V$

$R_C = V_{RC} / I_{CQ}$,

$= 10/4mA = 2.5k\Omega$

To find R_E: $I_{Csat} = V_{CC} / (R_C + R_E)$

To find R_B: Find I_B where, $I_B = I_C / \beta = 36.36\mu A$

Also, for an emitter bias circuit,

$I_B = (V_{CC} - V_{BE}) / R_B + (\beta + 1) R_E$

Thus, $R_B = 639.8\ k\Omega$

Standard values: $R_C = 2.4\ k\Omega$, $R_E = 1\ k\Omega$, $R_B = 620\ k\Omega$

$8mA = 28 / (2.5k + R_E)$

Thus, $R_E = 1k\Omega$

Transistor switching networks:

Through proper design transistors can be used as switches for computer and control applications.
When the input voltage V_B is high (logic 1), the transistor is in saturation (ON). And the output at its collector = V_{CE} is almost 0V(Logic 0)

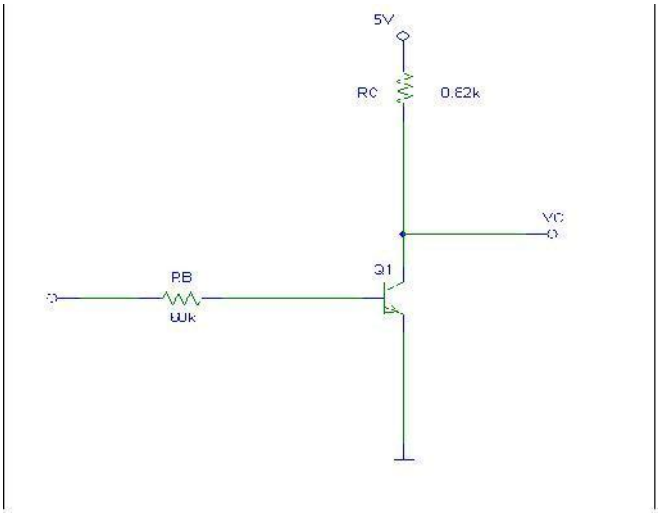
Transistor as a switch

When the base voltage V_B is low(logic 0), i.e, 0V, the transistor is cutoff(Off) and I_C is 0, drop across R_C is 0 and therefore voltage at the collector is V_{CC}.(logic 1)
Thus transistor switch operates as an inverter.
This circuit does not require any DC bias at the base of the transistor.

Design

When Vi (V_B) is 5V, transistor is in saturation and
I_{Csat} Just before saturation, $I_{B,max} = I_{C,sat} / \beta_{DC}$
Thus the base current must be greater than $I_{B,max}$ to make the transistor to work in saturation.

Analysis



When Vi = 5V, the resulting level of I_B is

$$I_B = (Vi - 0.7) / R_B$$

$= (5 – 0.7) / 68k$

$= 63\mu A$

$I_{Csat} = V_{CC} / R_C = 5/0.82k$

$= 6.1mA$

Verification

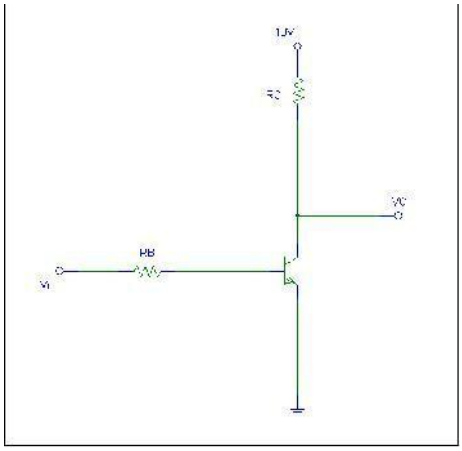
$(I_{C,sat} / \beta) = 48.8\mu A$

Thus $I_B > (I_{C,sat} / \beta)$ which is required for a transistor to be in saturation.

A transistor can be replaced by a low resistance Rsat when in saturation (switch on)
$R_{sat} = V_{CE\ sat} / I_{Csat}$ ($V_{CE\ sat}$ is very small and I_{Csat} is $I_{C,max}$ is maximum current)
A transistor can be replaced by a high resistance Rcutoff when in cutoff (switch on)

Problem

Determine R_B and R_C for the inverter of figure:



$I_{C\ sat} = V_{CC} / R_C$

$10mA = 10V / R_C$

$R_C = 1k\Omega$

I_B just at saturation $= I_{C\ sat} / \beta$

$= 10mA / 250$

$= 40\mu A$

Choose $I_B > I_{C\ sat} / \beta$, 60 μA

$I_B = (Vi – 0.7) / R_B$

$60\ \mu A = (10 – 0.7) / R_B$

$R_B = 155k\Omega$

Choose $R_B = 150k\Omega$, standard value,

re calculate I_B, we get $I_B = 62\ \mu A$ which is also > $I_{C\ sat} / \beta$

Thus, $R_C = 1k$ and $R_B = 155k$

Switching Transistors

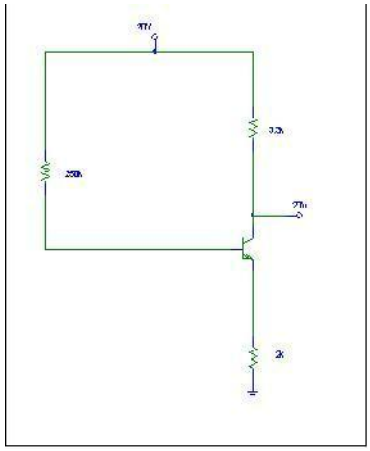
Transistor 'ON' time = delay time + Rise time
Delay time is the time between the changing state of the input and the beginning of a response at the output.
Rise time is the time from 10% to 90% of the final value.
Transistor 'OFF' time = Storage time + Fall time
For an 'ON' transistor, V_{BE} should be around 0.7V
For the transistor to be in active region, V_{CE} is usually about 25% to 75% of V_{CC}. If V_{CE} = almost V_{CC}, probable faults:

- the device is damaged
- connection in the collector – emitter or base – emitter circuit loop is open.

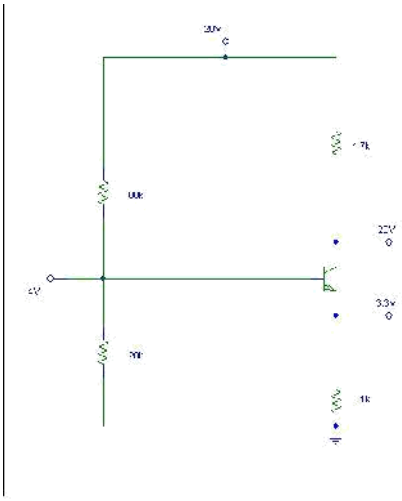
One of the most common mistake in the lab is usage of wrong resistor value. Check various voltages with respect to ground.
Calculate the current values using voltage readings rather than measuring current by breaking the circuit.

Problem – 1

Check the fault in the circuit given.



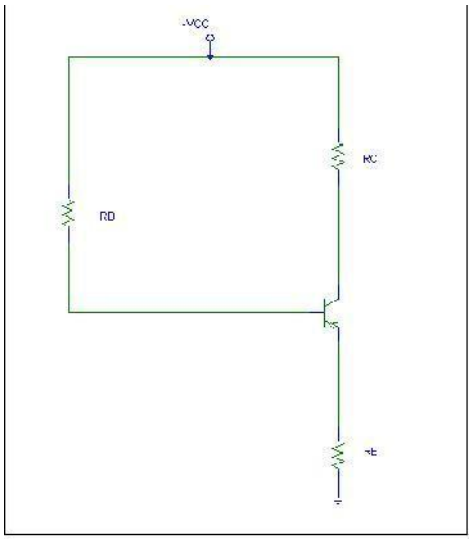
Problem - 2



PNP transistors

The analysis of PNP transistors follows the same pattern established for NPN transistors. The only difference between the resulting equations for a network in which an npn transistor has been replaced by a pnp transistor is the sign associated with particular quantities.

PNP transistor in an emitter bias



Applying KVL to Input loop:

$V_{CC} = I_B R_B + V_{BE} + I_E R_E$

Thus, $I_B = (V_{CC} - V_{BE}) / [R_B + (\beta+1) R_E]$

Applying KVL Output loop:

$V_{CE} = - (V_{CC} - I_C R_C)$

Bias stabilization

The stability of a system is a measure of the sensitivity of a network to variations in its parameters.

In any amplifier employing a transistor the collector current I_C is sensitive to each of the following parameters.

β increases with increase in temperature.

Magnitude of V_{BE} decreases about 2.5mV per degree Celsius increase in temperature.

I_{CO} doubles in value for every 10 degree Celsius increase in temperature.

T (degree Celsius)	Ico (nA)	β	V_{BE} (V)
- 65	0.2 x 10-3	20	0.85
25	0.1	50	0.65
100	20	80	0.48
175	3.3 x 103	120	0.3

Stability factors

$S (I_{CO}) = \Delta I_C / \Delta I_{C0}$

$S (V_{BE}) = \Delta I_C / \Delta V_{BE}$

$S (\beta) = \Delta I_C / \Delta \beta$

Networks that are quite stable and relatively insensitive to temperature variations have low stability factors.

The higher the stability factor, the more sensitive is the network to variations in that parameter.

S(I_{CO})

- Analyze S(I_{CO}) for
  - emitter bias configuration
  - fixed bias configuration
  - Voltage divider configuration

For the emitter bias configuration,

$S(I_{CO}) = (\beta + 1)[1 + R_B / R_E] / [(\beta + 1) + R_B /$

$R_E]$ If $R_B / R_E >> (\beta + 1)$, then

$S(I_{CO}) = (\beta + 1)$

For $R_B / R_E << 1$, $S(I_{CO})$ 1

Thus, emitter bias configuration is quite stable when the ratio R_B / R_E is as small as possible.
Emitter bias configuration is least stable when R_B / R_E approaches $(\beta + 1)$.

Fixed bias configuration

$S(I_{CO}) = (\beta + 1)[1 + R_B / R_E] / [(\beta + 1) + R_B /$

$R_E] = (\beta + 1)[R_E + R_B] / [(\beta + 1) R_E + R_B]$

By plugging $R_E = 0$, we get

$S(I_{CO}) = \beta + 1$

This indicates poor stability.

Voltage divider configuration

$S(I_{CO}) = (\beta + 1)[1 + R_B / R_E] / [(\beta + 1) + R_B /$

$R_E]$ Here, replace R_B with R_{th}

$S(I_{CO}) = (\beta + 1)[1 + R_{th} / R_E] / [(\beta + 1) + R_{th} / R_E]$

Thus, voltage divider bias configuration is quite stable when the ratio R_{th} / R_E is as small as possible.

Physical impact

In a **fixed bias circuit**, I_C increases due to increase in I_{C0}. [$I_C = \beta I_B + (\beta+1) I_{C0}$] I_B is fixed by V_{CC} and R_B. Thus level of I_C would continue to rise with temperature – a very unstable situation.

In **emitter bias circuit**, **as I_C increases**, I_E increases, V_E increases. Increase in V_E reduces I_B. $I_B = [V_{CC} - V_{BE} - V_E] / R_B$. A drop in I_B **reduces I_C**.Thus, this configuration is such that there is a reaction to an increase in I_C that will tend to oppose the change in bias conditions.

In the **DC bias with voltage feedback**, as I_C increases, voltage across R_C increases, thus reducing I_B and causing I_C to reduce.

The most stable configuration is **the voltage – divider network**. If the condition $\beta R_E >> 10R_2$, the voltage V_B will remain fairly constant for changing levels of I_C. $V_{BE} = V_B - V_E$, as I_C increases, V_E increases, since V_B is constant, V_{BE} drops making I_B to fall, which will try to offset the increases level of I_C.

$S(V_{BE})$

$S(V_{BE}) = \Delta I_C / \Delta V_{BE}$

For an emitter bias circuit, $S(V_{BE}) = - \beta / [R_B + (\beta + 1)R_E]$

If $R_E = 0$ in the above equation, we get $S(V_{BE})$ for a fixed bias circuit as, $S(V_{BE}) = - \beta / R_B$.

For an emitter bias,

$S(V_{BE}) = - \beta / [R_B + (\beta + 1)R_E]$ can be rewritten as,

$S(V_{BE}) = - (\beta/R_E)/ [R_B/R_E + (\beta + 1)]$

If $(\beta + 1) >> R_B/R_E$, then

$$S(V_{BE}) = - (\beta/R_E)/ (\beta + 1) = - 1/ R_E$$

The larger the R_E, lower the $S(V_{BE})$ and more stable is the system.

Total effect of all the three parameters on I_C can be written as,

$$\mathbf{\Delta I_C = S(I_{CO})\ \Delta I_{CO} + S(V_{BE})\ \Delta V_{BE} + S(\beta)\Delta\beta}$$

General conclusion:

The ratio R_B / R_E or R_{th} / R_E should be as small as possible considering all aspects of design.

Transistor at low frequencies

- Introduction
- Amplification in the AC domain
- BJT transistor modeling
- The re Transistor Model
- The Hybrid equivalent Model

Introduction

- There are three models commonly used in the small – signal ac analysis of transistor networks:
- The re model
- The hybrid π model
- The hybrid equivalent model

Amplification in the AC domain

The transistor can be employed as an amplifying device, that is, the output ac power is greater than the input ac power. The factor that permits an ac power output greater than the input ac power is the applied DC power. The amplifier is initially biased for the required DC voltages and currents. Then the ac to be amplified is given as input to the amplifier. If the applied ac exceeds the limit set by dc level, clipping of the peak region will result in the output. Thus, proper (faithful) amplification design requires that the dc and ac components be sensitive to each other's requirements and limitations. The superposition theorem is applicable for the analysis and design of the dc and ac components of a BJT network, permitting the separation of the analysis of the dc and ac responses of the system.

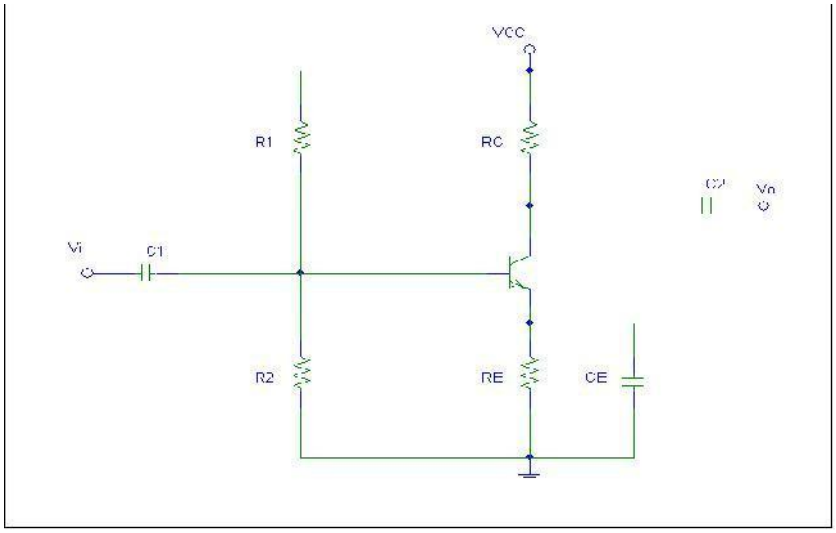
BJT Transistor modeling

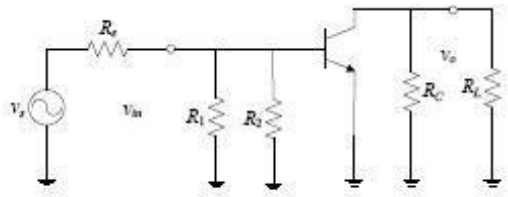
- The key to transistor small-signal analysis is the use of the equivalent circuits (models). **A MODEL IS A COMBINATION OF CIRCUIT ELEMENTS LIKE VOLTAGE OR CURRENT SOURCES, RESISTORS, CAPACITORS** etc, that best approximates the behavior of a device under specific operating conditions. Once the model (ac equivalent circuit) is determined, the schematic symbol for the device can be replaced by the equivalent circuit and the basic methods of circuit analysis applied to determine the desired quantities of the network.
- Hybrid equivalent network – employed initially. Drawback – It is defined for a set of operating conditions that might not match the actual operating conditions.
- re model: desirable, but does not include feedback term

- Hybrid π model: model of choice.

AC equivalent of a network

- AC equivalent of a network is obtained by:
- Setting all dc sources to zero and replacing them by a short – circuit equivalent
- Replacing all capacitors by short – circuit equivalent
- Removing all elements bypassed by the short – circuit equivalents
- Redrawing the network in a more convenient and logical form.



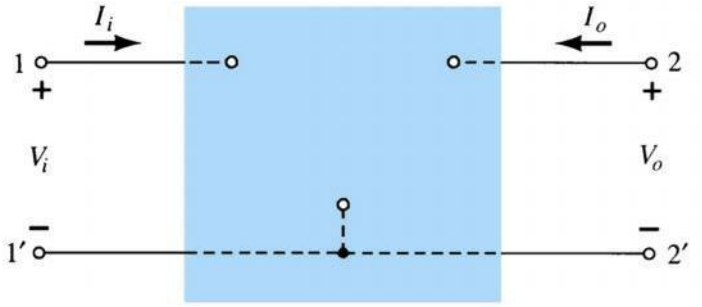


r_e model

- In r_e model, the transistor action has been replaced by a single diode between emitter and base terminals and a controlled current source between base and collector terminals.
- This is rather a simple equivalent circuit for a device

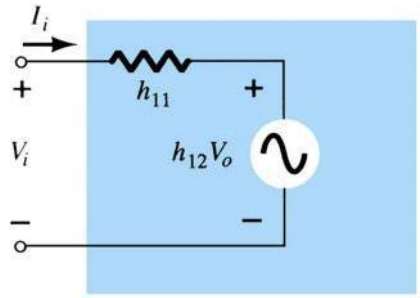
The Hybrid equivalent model

- For the hybrid equivalent model, the parameters are defined at an operating point.
- The quantities h_{ie}, h_{re},h_{fe}, and h_{oe} are called hybrid parameters and are the components of a small – signal equivalent circuit.
- The description of the hybrid equivalent model will begin with the general two port system.

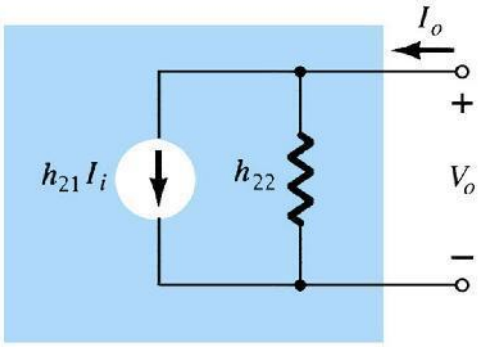


- The set of equations in which the four variables can be related are:
- $V_i = h_{11}I_i + h_{12}V_o$
- $I_o = h_{21}I_i + h_{22}V_o$
- The four variables h_{11}, h_{12}, h_{21} and h_{22} are called hybrid parameters (the mixture of variables in each equation results in a " hybrid" set of units of measurement for the h – parameters.
- Set $V_o = 0$, solving for h_{11}, $h_{11} = V_i / I_i$ Ohms
- This is the ratio of input voltage to the input current with the output terminals shorted. It is called Short circuit input impedance parameter.
- If I_i is set equal to zero by opening the input leads, we get expression for h_{12}: $h_{12} = V_i / V_o$, This is called open circuit reverse voltage ratio.
- Again by setting V_o to zero by shorting the output terminals, we get $h_{21} = I_o / I_i$ known as short circuit forward transfer current ratio.
- Again by setting $I_1 = 0$ by opening the input leads, $h_{22} = I_o / V_o$. This is known as open – circuit output admittance. This is represented as resistor ($1/h_{22}$)
    - $h_{11} = h_i$ = input resistance
    - $h_{12} = h_r$ = reverse transfer voltage ratio
    - $h_{21} = h_f$ = forward transfer current ratio
    - $h_{22} = h_o$ = Output conductance

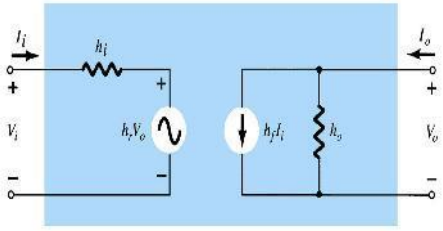
Hybrid Input equivalent circuit



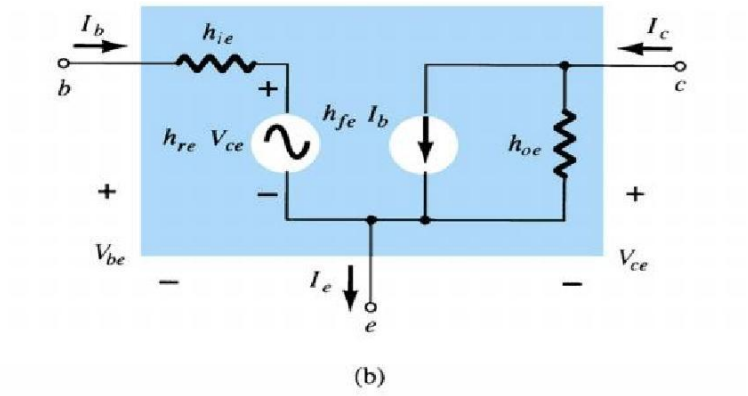
Hybrid output equivalent circuit



Complete hybrid equivalent circuit



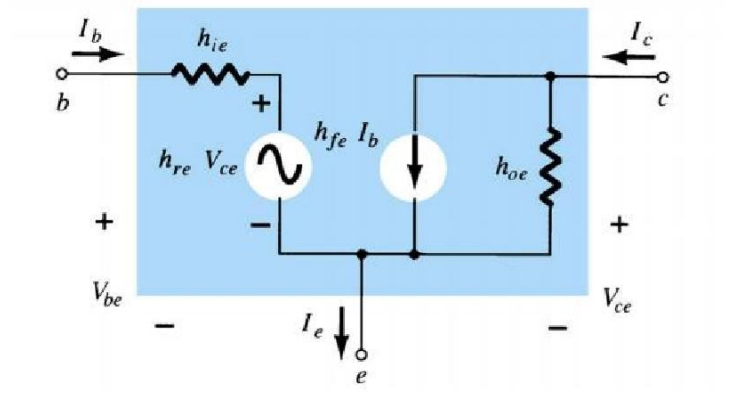
Common Emitter Configuration - hybrid equivalent circuit



(b)

- Essentially, the transistor model is a three terminal two – port system.
- The h – parameters, however, will change with each configuration.
- To distinguish which parameter has been used or which is available, a second subscript has been added to the h – parameter notation.
- For the common – base configuration, the lowercase letter b is added, and for common emitter and common collector configurations, the letters e and c are used respectively.

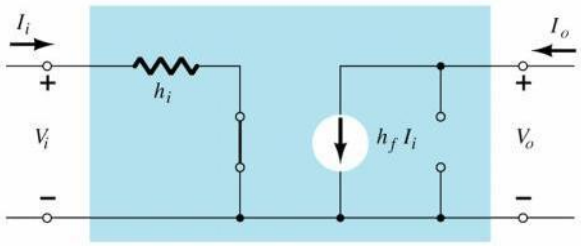
Common Base configuration - hybrid equivalent circuit

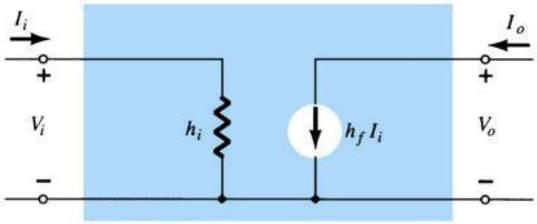


(b)

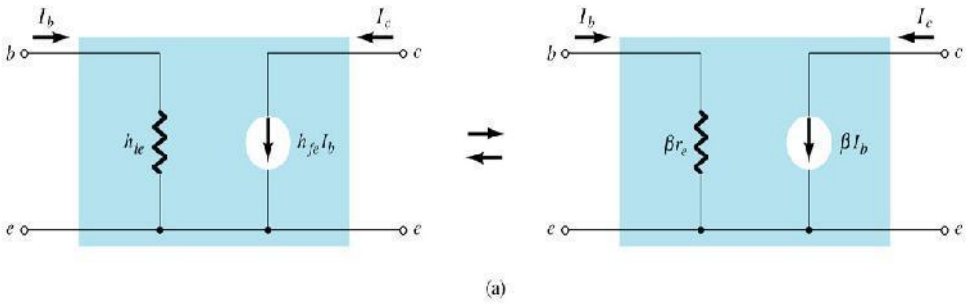
Configuration	**I_i**	**I_o**	**V_i**	**V_o**
Common emitter	**I_b**	**I_c**	**V_{be}**	**V_{ce}**
Common base	**I_e**	**I_c**	**V_{eb}**	**V_{cb}**
Common Collector	**I_b**	**I_e**	**V_{be}**	**V_{ec}**

- Normally h_r is a relatively small quantity, its removal is approximated by $h_r \cong 0$ and $h_r V_o = 0$, resulting in a short – circuit equivalent.
- The resistance determined by $1/h_o$ is often large enough to be ignored in comparison to a parallel load, permitting its replacement by an open – circuit equivalent.





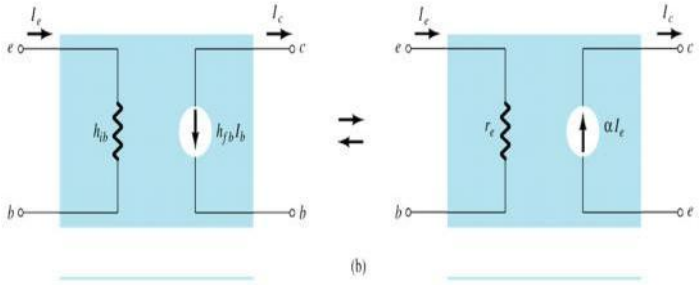
h-Parameter Model v/s. r_e Model



$$h_{ie} = \beta r_e$$

$$h_{fe} = \beta_{ac}$$

Common Base: r_e v/s. h-Parameter Model



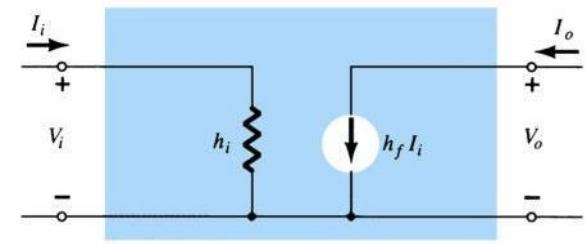
Common-Base configurations - h-Parameters

$$h_{ib} = r_e$$

$$h_{fb} = - \alpha = -1$$

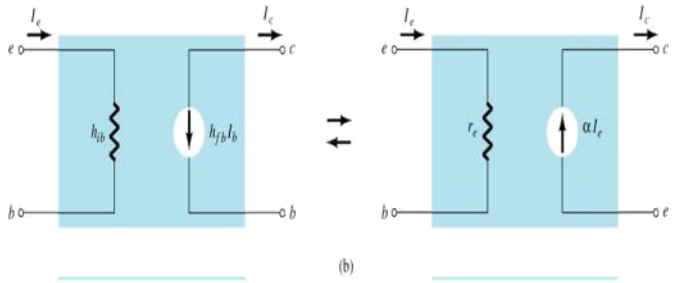
Problem

- Given $I_E = 3.2mA$, $h_{fe} = 150$, $h_{oe} = 25\mu S$ and $h_{ob} = 0.5\ \mu S$. Determine
  - The common – emitter hybrid equivalent
  - The common – base r_e model



Solution:

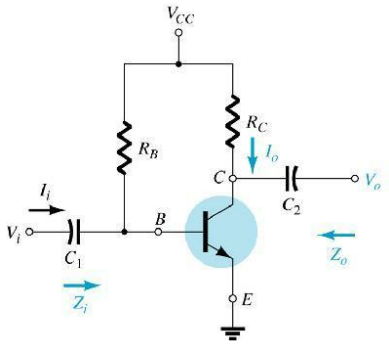
- We know that, $h_{ie} = \beta_{re}$ and $r_e = 26mV/I_E = 26mV/3.2mA = 8.125\Omega$
- $\beta_{re} = (150)(8.125) = 1218.75k\Omega$
- $r_o = 1/h_{oe} = 1/25\mu S = 40k\Omega$



- $r_e = 8.125\Omega$
- $r_o = 1/ h_{ob} = 1/0.5\mu S = 2M\ \Omega$
- $\alpha \cong 1$

- Small signal ac analysis includes determining the expressions for the following parameters in terms of Z_i, Z_o and A_V in terms of
  - β
  - r_e
  - r_o and
  - R_B, R_C
- Also, finding the phase relation between input and output
- The values of β, r_o are found in datasheet
- The value of r_e must be determined in dc condition as $r_e = 26mV / I_E$

Common Emitter - Fixed bias configuration



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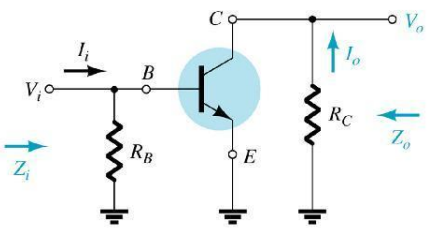
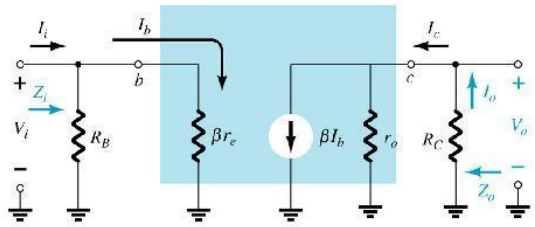
Removing DC effects of V_{CC} and Capacitors



r_e model



Small signal analysis – fixed bias

- From the above re model,

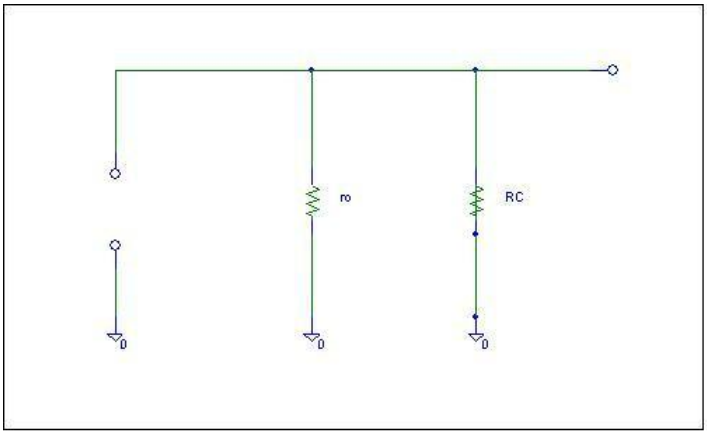
$$Z_i = [R_B \,||\, \beta r_e] \text{ ohms}$$

If $R_B > 10\ \beta r_e$, then,

$$[R_B \,||\, \beta r_e] \cong \beta r_e$$

Then, $Z_i \cong \beta r_e$

- Z_o is the output impedance when $V_i = 0$. When $V_i = 0$, $i_b = 0$, resulting in open circuit equivalence for the current source.



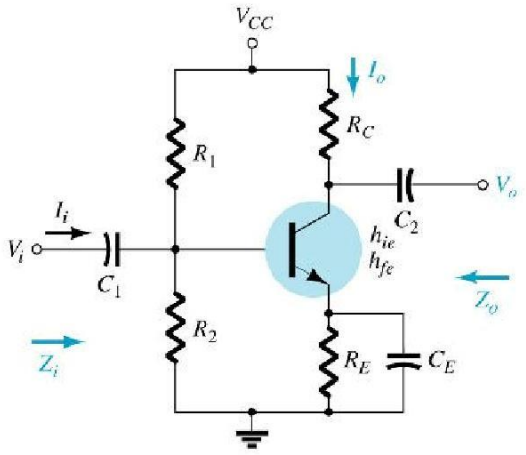
- $Z_o = [R_C \,||\, r_o]$ ohms
- A_V
  - $V_o = - \beta I_b (R_C \,||\, r_o)$

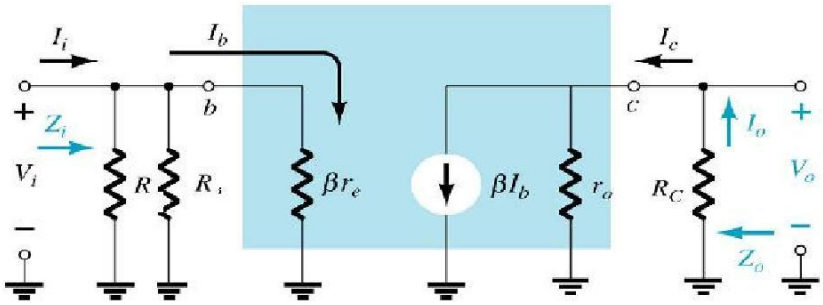
- From the r_e model, $I_b = V_i / \beta\ r_e$
- thus,
  - $V_o = - \beta\ (V_i / \beta\ r_e)\ (R_C \,||\, r_o)$
  - $A_V = V_o / V_i = - (R_C \,||\, r_o) / r_e$

If $r_o > 10R_C$,

- $A_V = -(R_C / r_e)$ egative sign in the gain expression indicates that there exists 180o phase shift between the input and output.

Common Emitter - Voltage-Divider Configuration





- The r_e model is very similar to the fixed bias circuit except for R_B is $R_1 \,||\, R_2$ in the case of voltage divider bias.
- Expression for A_V remains the same.

$$Z_i = R_1 \,||\, R_2 \,||\, \beta r_e$$
$$Z_o = R_C$$

- From the r_e model, $I_b = V_i / \beta r_e$
- thus,

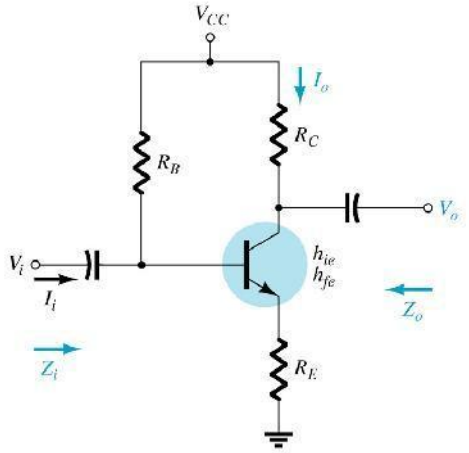
$$V_o = -\beta (V_i / \beta r_e)(R_C \,||\, r_o)$$

- $$A_V = V_o / V_i = -(R_C \,||\, r_o) / r_e$$

- If r_o >10R_C,

$$A_V = - (R_C / r_e)$$

Common Emitter - Unbypassed Emitter-Bias Configuration



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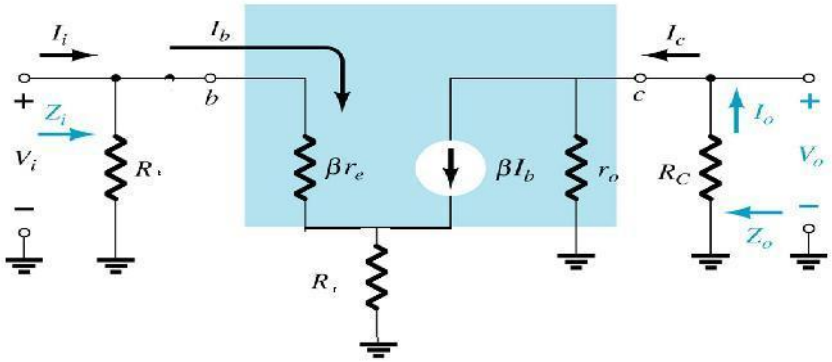


- Applying KVL to the input side:

$$V_i = I_b \beta r_e + I_e R_E$$

$$V_i = I_b \beta r_e + (\beta + 1) I_b R_E$$

Input impedance looking into the network to the right of RB is

$$Z_b = V_i / I_b = \beta r_e + (\beta + 1) R_E$$

Since $\beta >> 1$, $(\beta + 1) = \beta$

Thus,

$$Z_b = V_i / I_b = \beta (r_e + R_E)$$

- Since R_E is often much greater than r_e,

$$Z_b = \beta R_E,$$

-

$$Z_i = R_B \| Z_b$$

- Z_o is determined by setting V_i to zero, $I_b = 0$ and βI_b can be replaced by open circuit equivalent. The result is,

\endash $Z_o = R_C$

- A_V : We know that, $V_o = - I_o R_C$

$$- \beta I_b R_C$$

$$- \beta (V_i / Z_b) R_C$$

$$A_V = V_o / V_i = - \beta (R_C / Z_b)$$

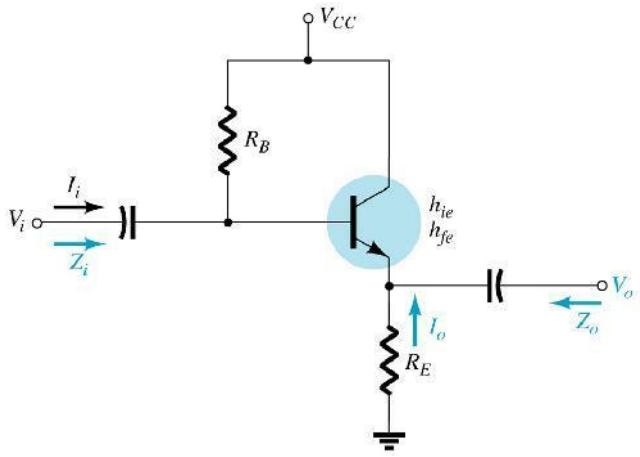
Substituting, $Z_b = \beta (r_e + R_E)$

$$A_V = V_o / V_i = - \beta [R_C / (r_e + R_E)]$$

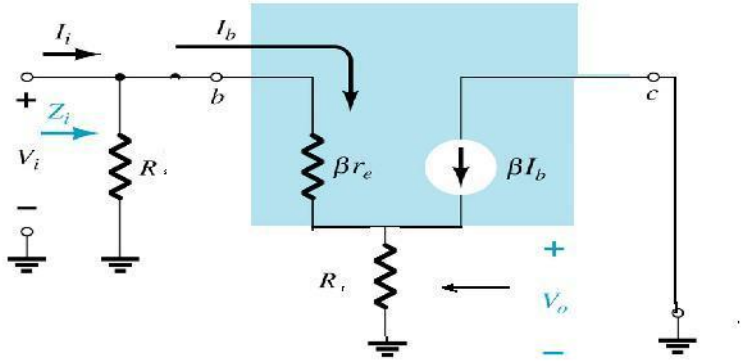
$R_E >> r_e$, $A_V = V_o / V_i = - \beta [R_C / R_E]$

- Phase relation: The negative sign in the gain equation reveals a 180^o phase shift between input and output.

Emitter – follower



r_e model



- $Z_i = R_B \parallel Z_b$
- $Z_b = \beta r_e + (\beta + 1)R_E$
- $Z_b = \beta(r_e + R_E)$
- Since R_E is often much greater than r_e, $Z_b = \beta R_E$
- To find Zo, it is required to find output equivalent circuit of the emitter follower at its input terminal.
- This can be done by writing the equation for the current Ib.

$$I_b = V_i / Z_b$$

$$I_e = (\beta + 1)I_b$$

$$= (\beta + 1)(V_i / Z_b)$$

- We know that, $Z_b = \beta r_e + (\beta + 1)R_E$ substituting this in the equation for Ie we get,

$$I_e = (\beta +1)\ (V_i / Z_b)$$

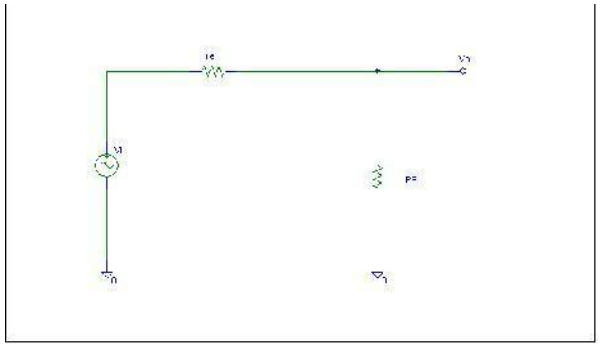
$$= (\beta +1)\ (V_i / \beta r_e + (\beta +1)R_E\ )$$

$$I_e = V_i / [\beta r_e / (\beta +1)] + R_E$$

- Since $(\beta +1) = \beta$,

$$I_e = V_i / [r_e + R_E]$$

- Using the equation $I_e = V_i / [r_e + R_E]$, we can write the output equivalent circuit as,

- 

- As per the equivalent circuit,

$$Z_o = R_E \| r_e$$

- Since R_E is typically much greater than r_e, $Z_o \cong r_e$
- A_V – Voltage gain:
- Using voltage divider rule for the equivalent circuit,

$$V_o = V_i\ R_E / (R_E + r_e)$$

$$A_V = V_o / V_i\ = [R_E / (R_E + r_e)]$$

- Since $(R_E + r_e) \cong R_E$,

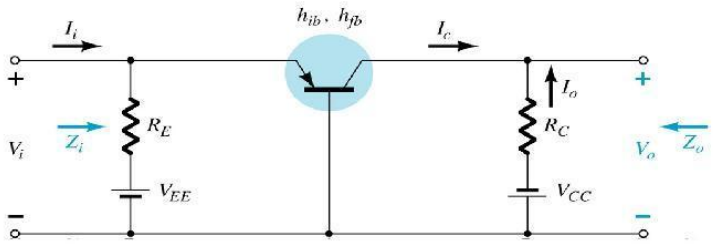
$$A_V \cong [R_E / (R_E] \cong 1$$

-

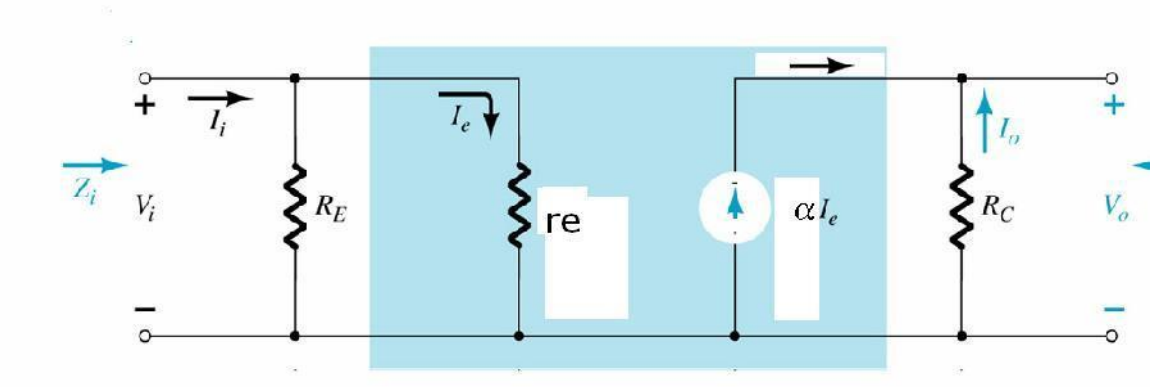
- Phase relationship

As seen in the gain equation, output and input are in phase.

Common base configuration



r_e model



Small signal analysis

- Input Impedance: $Z_i = R_E \| r_e$
- Output Impedance: $Z_o = R_C$

5. To find, Output voltage,

$$V_o = - I_o R_C$$

$$V_o = - (-I_C) R_C = \alpha I_e R_C$$

- $I_e = V_i / r_e$, substituting this in the above equation, $V_o = \alpha (V_i / r_e) R_C$

$$V_o = \alpha (V_i / r_e) R_C$$

Voltage Gain: A_V:

$$A_V = V_o / V_i = \alpha (R_C / r_e)$$

$\alpha \cong 1$; $A_V = (R_C / r_e)$

Current gain

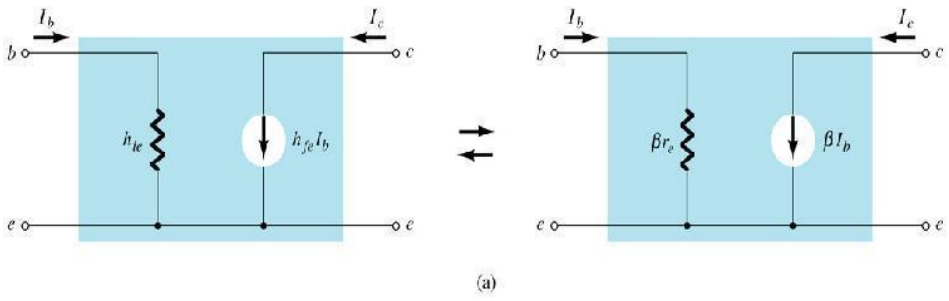
$$A_i = I_o / I_i$$

$$I_o = - \alpha I_e = - \alpha I_i$$

$$I_o / I_i = - \alpha \cong -1$$

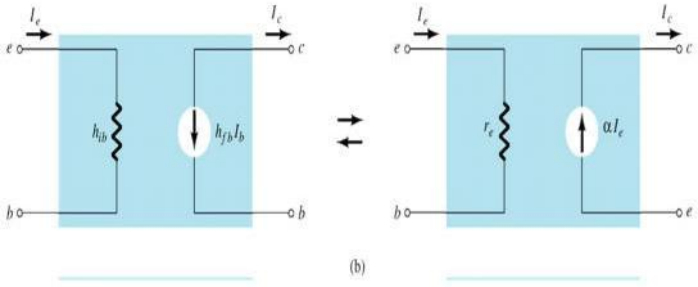
Phase relation: Output and input are in phase.

- **h-Parameter Model vs. re Model**



(a)

- **CB re vs. h-Parameter Model**



(b)

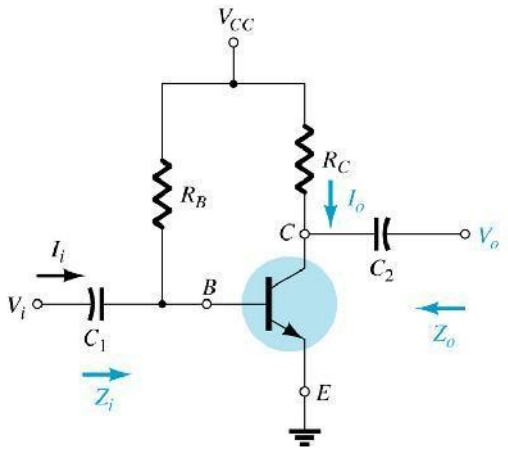
Common-Base h-Parameters

$$h_{ib} = r_e$$

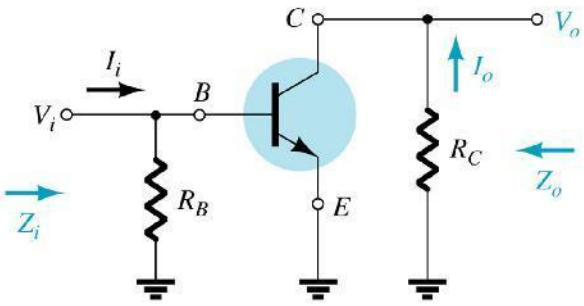
$$h_{fb} = -\alpha \cong -1$$

- Small signal ac analysis includes determining the expressions for the following parameters in terms of Z_i, Z_o and A_V in terms of
  - β
  - r_e
  - r_o and
  - R_B, R_C
- Also, finding the phase relation between input and output
- The values of β, r_o are found in datasheet
- The value of re must be determined in dc condition as $r_e = 26mV / I_E$

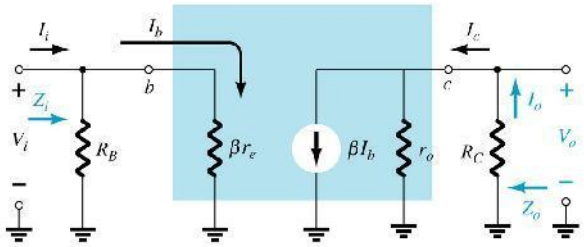
Common Emitter Fixed bias configuration



Removing DC effects of V_{CC} and Capacitors



r_e model



Small signal analysis – fixed bias

Input impedance Z_i:

From the above r_e model, is,

$$Z_i = [R_B \,||\, \beta r_e] \text{ ohms}$$

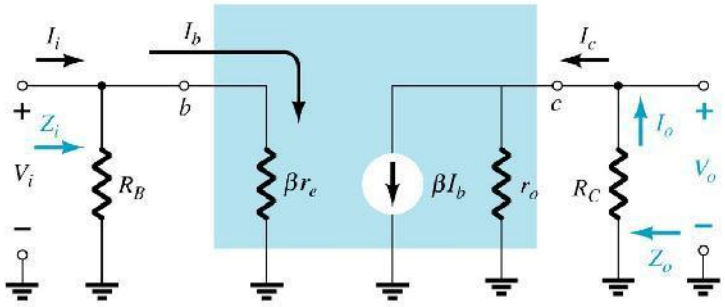
If $R_B > 10\ \beta r_e$, then,

$$[RB \,||\, \beta r_e] \cong \beta r_e$$

Then, $\mathbf{Z_i \cong \beta r_e}$

Ouput impedance Z_{oi}:

Z_o is the output impedance when $V_i = 0$. When $V_i = 0$, $i_b = 0$, resulting in open circuit equivalence for the current source.



$$\mathbf{Z_o = [R_C \,||\, r_o\,] \text{ ohms}}$$

Voltage Gain A_v:

$$V_o = - \beta I_b (R_C \parallel r_o)$$

From the re model, $I_b = V_i / \beta r_e$

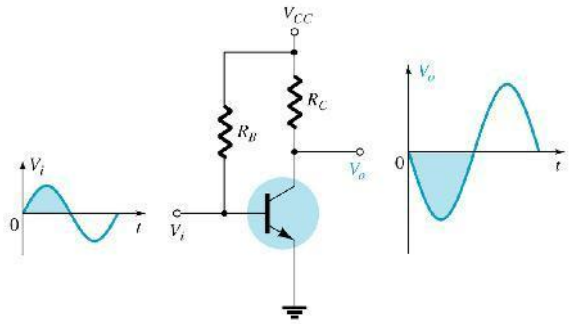
thus, $V_o = - \beta (V_i / \beta r_e) (R_C \parallel r_o)$

$$A_V = V_o / V_i = - (R_C \parallel r_o) / r_e$$

If $r_o > 10R_C$, $\mathbf{A_V = - (R_C / r_e)}$

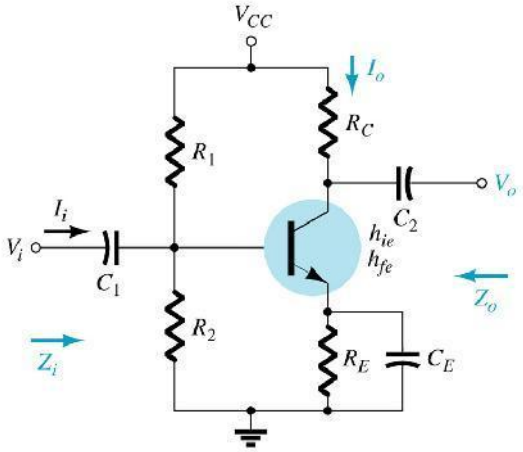
Phase Shift:

The negative sign in the gain expression indicates that there exists 180^o phase shift between the input and output.

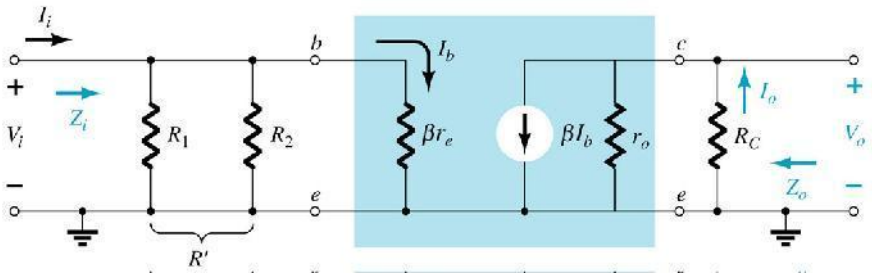


Problem:

Common Emitter - Voltage-Divider Configuration



Equivalent Circuit:



The re model is very similar to the fixed bias circuit except for R_B is $R_1 \,||\, R_2$ in the case of voltage divider bias.

Expression for A_V remains the same.

$Z_i = R_1 \,||\, R_2 \,||\, \beta\, r_e$

$Z_o = R_C$

:

Voltage Gain, A_V:

From the r_e model,

$$I_b = V_i / \beta\, r_e$$

$$V_o = - I_o\, (R_C \,||\, r_o),$$

$$I_o = \beta\, I_b$$

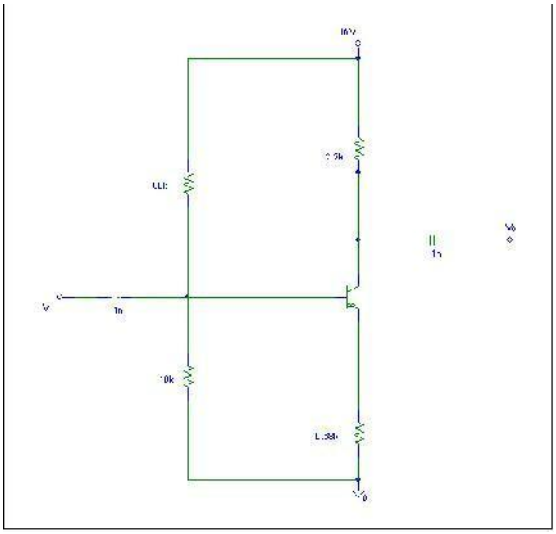
thus, $$V_o = - \beta\, (V_i / \beta\, r_e)\, (R_C \,||\, r_o)$$

$$A_V = V_o / V_i = - (R_C \,||\, r_o) / r_e$$

If $r_o > 10R_C$, $$A_V = - (R_C / r_e)$$

Problem:

Given: $\beta = 210$, $r_o = 50k\Omega$.
Determine: r_e, Z_i, Z_o, A_V. For the network given:



To perform DC analysis, we need to find out whether to choose exact analysis or approximate analysis.

This is done by checking whether $\beta R_E > 10R_2$, if so, approximate analysis can be chosen.

Here, $\beta R_E = (210)(0.68k) = 142.8k\Omega$.

$10R2 = (10)(10k) = 100k$.

Thus, $\beta RE > 10R2$.

Therefore using **approximate analysis,**

$$V_B = V_{cc}R_2 / (R_1+R_2)$$

$$= (16)(10k) / (90k+10k) = 1.6V$$

$$V_E = V_B - 0.7 = 1.6 - 0.7 = 0.9V$$

$$I_E = V_E / R_E = 1.324mA$$

$$r_e = 26mV / 1.324mA = 19.64\Omega$$

Effect of r_o can be neglected if $r_o \geq 10(R_C)$. In the given circuit, $10R_C$ is 22k, r_o is 50K.

Thus effect of r_o can be neglected.

$$Z_i = (R_1||R_2||\beta R_E)$$

$$= [90k||10k||(210)(0.68k)] =$$

$8.47k\Omega$ $Z_o = R_C = 2.2\ k\Omega$

$$A_V = - R_C / R_E = - 3.24$$

If the same circuit is with emitter resistor bypassed,

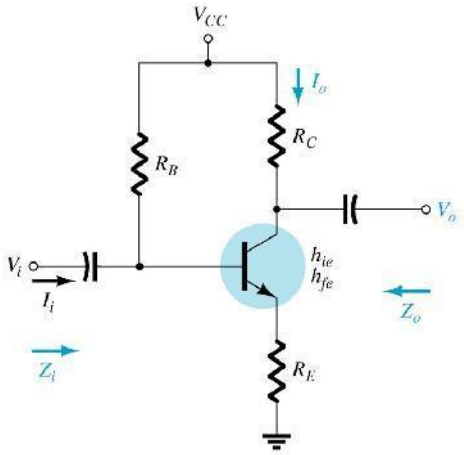
Then value of re remains same.

$$Z_i = (R_1||R_2||\beta r_e) = 2.83\ k\Omega$$

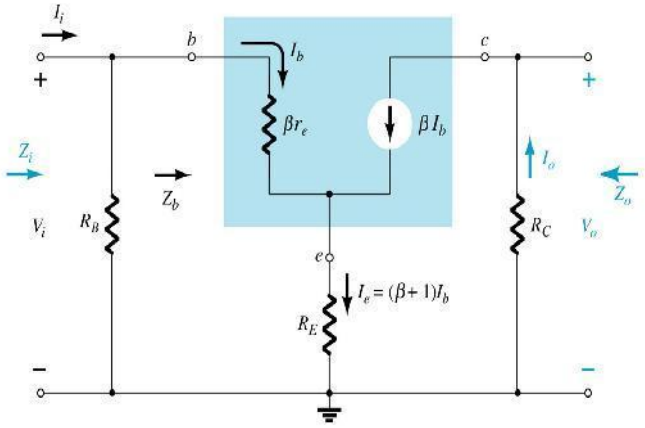
$$Z_o = R_C = 2.2\ k\Omega$$

$$A_V = - R_C / r_e = - 112.02$$

Common Emitter Un bypassed Emitter - Fixed Bias Configuration



Equivalent Circuit:



Applying KVL to the input side:

$$V_i = I_b\beta r_e + I_e R_E$$

$$V_i = I_b\beta r_e + (\beta + 1)\ I_b R_E$$

Input impedance looking into the network to the right of R_B is

$$Z_b = V_i / I_b = \beta r_e + (\beta + 1) R_E$$

Since $\beta >> 1$, $(\beta + 1) = \beta$

Thus, $Z_b = V_i / I_b = \beta (r_e + R_E)$

Since R_E is often much greater than r_e, Z_b

$= \beta R_E$, Z_i

$= R_B || Z_b$

Z_o is determined by setting V_i to zero, $I_b = 0$ and βI_b can be replaced by open circuit equivalent. The result is, We know that,

$Z_o = R_C$

$V_o = - I_o R_C$

$= - \beta I_b R_C$

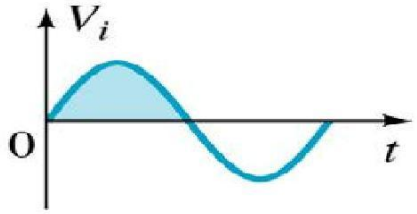
$= - \beta (V_i / Z_b) R_C$

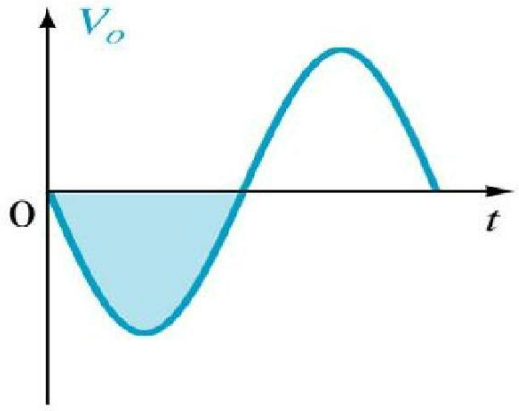
$A_V = V_o$ / V_i = - $\beta (R_C / Z_b)$ Z_b = $\beta (r_e + R_E)$

Substituting $R_E >> r_e$,

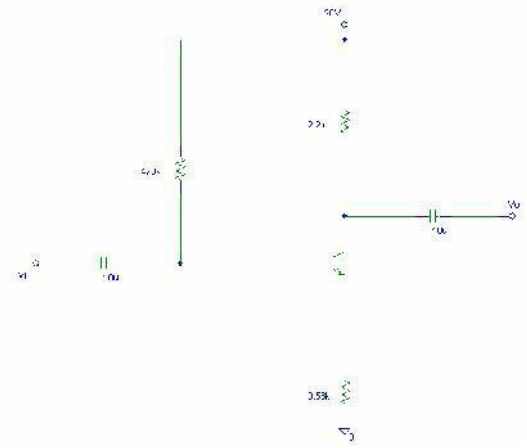
$A_V = V_o / V_i = - \beta [R_C / (r_e + R_E)]$ $A_V = V_o / V_i = - \beta [R_C / R_E]$

Phase relation: The negative sign in the gain equation reveals a 180^o phase shift between input and output.





Problem:



Given: $\beta = 120$, $r_o = 40k\Omega$.
Determine: r_e, Z_i, Z_o, A_V.
To find r_e, it is required to perform DC analysis and find I_E as $r_e = 26mV / I_E$ To find I_E, it is required to find I_B.

We know that,

$$I_B = (V_{CC} - V_{BE}) / [R_B + (\beta+1)R_E]$$

$$I_B = (20 - 0.7) / [470k + (120+1)0.56k] = 35.89\mu A$$

$$I_E = (\beta+1)I_B = 4.34mA$$

$$r_e = 26mV / I_E = 5.99\Omega$$

Effect of r_o can be neglected, if $r_o \geq 10(R_C + R_E)$

$$10(R_C + R_E) = 10(2.2\ k\Omega + 0.56k)$$

$$= 27.6\ k\Omega$$

and given that r_o is 40 kΩ, thus effect of r_o can be ignored.

$$Z_i = R_B || [\beta (r_e + R_E)]$$

$$= 470k || [120 (5.99 + 560)] = 59.34\Omega$$

$$Z_o = R_C = 2.2\ k\Omega$$

$$A_V = - \beta R_C / [\beta (r_e + R_E)]$$

$$= - 3.89$$

Analyzing the above circuit with Emitter resistor bypassed i.e., Common Emitter

$$I_B = (V_{CC} - V_{BE}) / [R_B + (\beta+1)R_E]$$

$$I_B = (20 - 0.7) / [470k + (120+1)0.56k] = 35.89\mu A$$

$I_E = (\beta+1)I_B = 4.34mA$

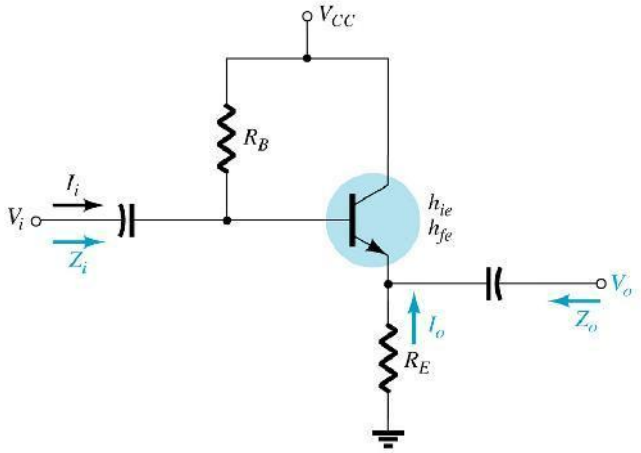
$r_e = 26mV / I_E = 5.99\Omega$

$Z_i = R_B \| [\beta r_e] = 717.70\Omega$

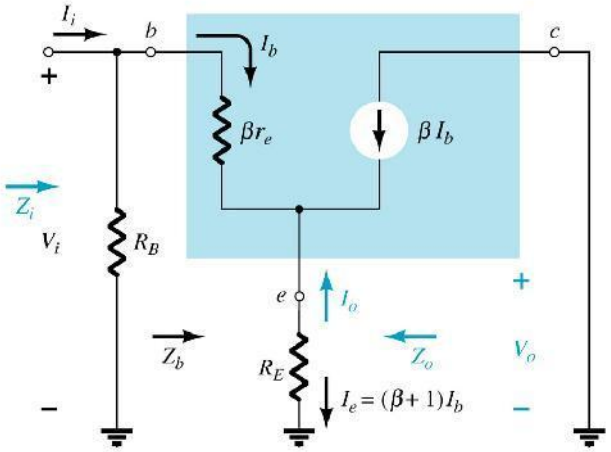
$Z_o = R_C = 2.2\ k\Omega$

$A_V = - R_C / r_e = - 367.28$ (a significant increase)

Emitter – follower



r_e model



$Z_i = R_B \| Z_b$

$Z_b = \beta r_e + (\beta + 1)R_E$

$Z_b = \beta(r_e + R_E)$

Since R_E is often much greater than r_e, $Z_b = \beta R_E$

To find Z_o, it is required to find output equivalent circuit of the emitter follower at its input terminal.

This can be done by writing the equation for the current

$$I_b.\ I_b = V_i / Z_b$$

$$I_e = (\beta +1)I_b$$

$$= (\beta +1)\ (V_i / Z_b)$$

We know that,

$$Z_b = \beta r_e + (\beta +1)R_E$$

substituting this in the equation for I_e we get,

$$I_e = (\beta +1)\ (V_i / Z_b)$$

$$= (\beta +1)\ (V_i / \beta r_e + (\beta +1)R_E\ )$$

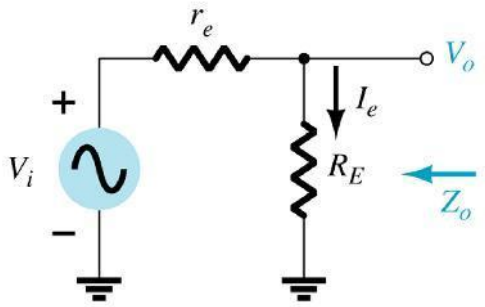
dividing by $(\beta +1)$, we get,

$$I_e = V_i / [\beta r_e / (\beta +1)] + R_E$$

Since $(\beta +1) = \beta$,

$$I_e = V_i / [r_e + R_E]$$

Using the equation $I_e = V_i / [r_e + R_E]$, we can write the output equivalent circuit as,



As per the equivalent circuit,

$$Z_o = R_E \| r_e$$

Since R_E is typically much greater than r_e,

$$Zo \cong re$$

A_V – Voltage gain:

Using voltage divider rule for the equivalent circuit, V_o

$$= V_i R_E / (R_E + r_e)$$

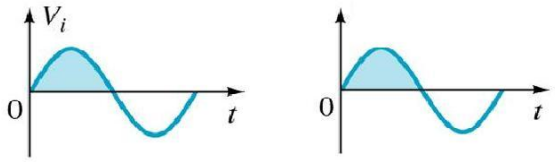
$$A_V = V_o / V_i = [R_E / (R_E + r_e)]$$

Since $(R_E + r_e) \cong R_E$,

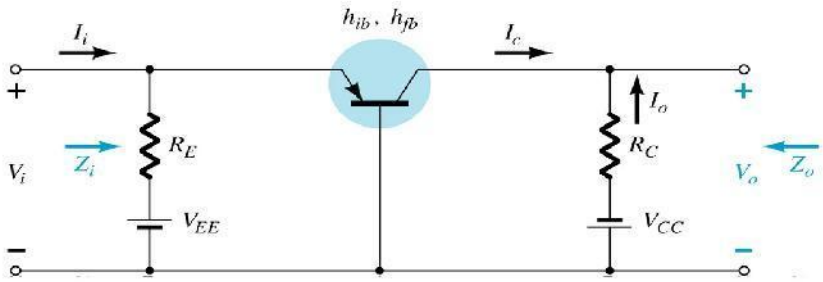
$$A_V \cong [R_E / (R_E] \cong 1$$

Phase relationship

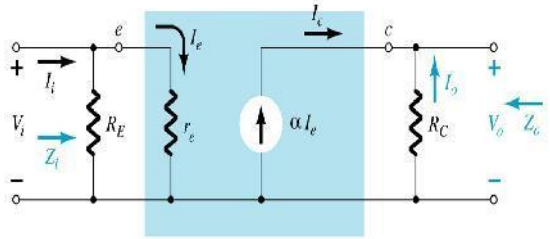
As seen in the gain equation, output and input are in phase.



Common base configuration



r_e model



Small signal analysis

$$Z_i = R_E \| r_e$$

$$Z_o = R_C$$

To find

$$V_o = - I_o R_C$$

$$V_o = - (-I_C) R_C = \alpha I_e R_C$$

Substituting this in the above equation, $I_e = V_i / r_e$,

$$V_o = \alpha (V_i / r_e) R_C$$

$$V_o = \alpha (V_i / r_e) R_C$$

$$A_V = V_o / V_i = \alpha (R_C / r_e)$$

$\alpha \cong 1$; $\quad A_V = (R_C / r_e)$

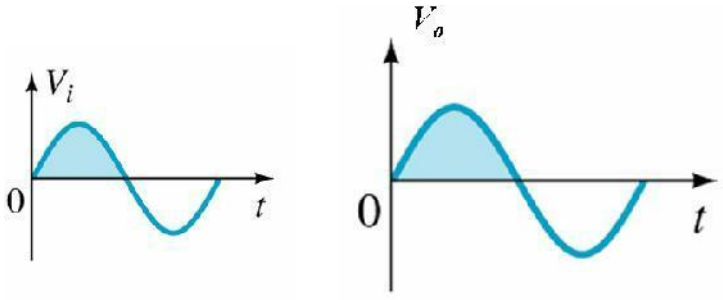
Current gain A_i :

$$A_i = I_o / I_i$$

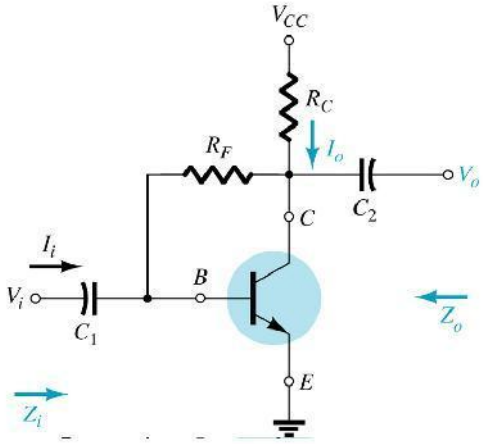
$$I_o = - \alpha I_e = - \alpha I_i$$

$$I_o / I_i = - \alpha \cong -1$$

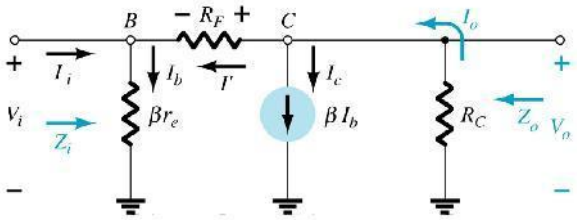
Phase relation: Output and input are in phase.



Common Emitter - Collector Feedback Configuration



r_e Model



Input Impedance: Z_i

$$Z_i = V_i / I_i,$$

$$I_i = I_b - I',$$

thus it is required to find expression for I' in terms of known resistors.

$$I' = (V_o - V_i)/ R_F \qquad (1)$$

$$V_o = - I_o R_C$$

$$I_o = \beta I_b + I'$$

Normally, $I' << \beta I_b$

thus, $I_o = \beta I_b$,

$$V_o = - I_o R_C$$

$$V_o = - \beta I_b R_C,$$

Replacing I_b by $V_i / \beta r_e$

Thus,

$$V_o = - \beta (V_i R_C) / \beta r_e$$

$$= - (V_i R_C) / r_e \qquad (2)$$

Substituting (2) in (1):

$$I' = (V_o - V_i)/ R_F$$

$$= (V_o / R_F) - (V_i/ R_F)$$

$$= - [(V_i R_C) / R_F r_e] - (V_i/ R_F)$$

$$I' = - V_i/R_F[(R_C / r_e)+1]$$

We know that, $V_i = I_b \beta r_e$,

$$I_b = I_i + I'$$

and, $$I' = - V_i/R_F[(R_C / r_e) +1]$$

Thus, $$V_i = (I_i + I') \beta r_e = I_i \beta r_e + I' \beta r_e$$

$$= I_i \beta r_e - (V_i \beta r_e)(1/R_F)[(R_C / r_e)+1]$$

Taking V_i terms on left side:

$$V_i + (V_i \beta r_e)(1/R_F)[(R_C / r_e)+1] = I_i \beta r_e$$

$$V_i[1 + (\beta r_e)(1/R_F)[(R_C / r_e) +1] = I_i \beta r_e$$

$$V_i / I_i = \beta r_e / [1 + (\beta r_e)(1/R_F)[(R_C / r_e) +1]$$

But, $[(R_C / r_e)+1] \cong R_C / r_e$

(because $R_C >> r_e$)

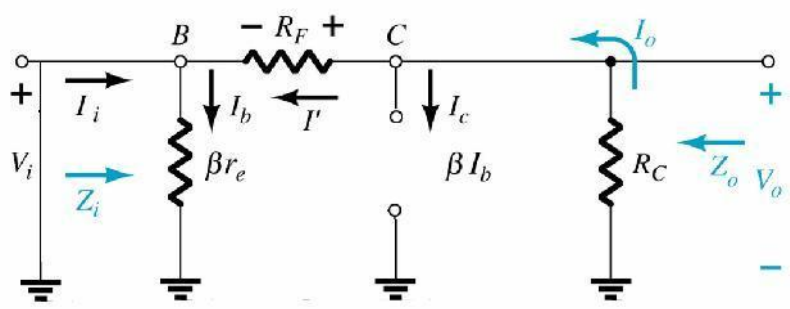
Thus, $$Z_i = V_i / I_i$$

$$= \beta r_e / [1 + (\beta r_e)(1/R_F)[(R_C / r_e)]$$

$$= \beta r_e / [1 + (\beta)(R_C/R_F)]$$

Thus, $$\mathbf{Z_i = r_e / [(1/\beta) + (R_C/R_F)]}$$

To find Output Impedance Zo:



$Z_o = R_C \parallel R_F$ (Note that $i_b = 0$, thus no effect of βr_e on Z_o)

Voltage Gain A_V:

$$V_o = - I_o R_C$$

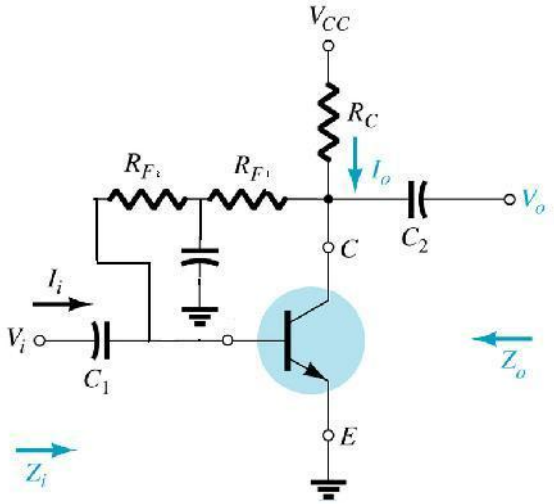
$$= - \beta I_b R_C \text{ (neglecting the value of I')}$$

$$= - \beta (V_i / \beta r_e) R_C$$

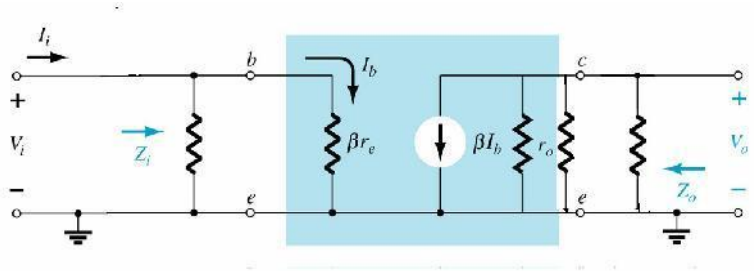
$$A_V = V_o / V_i = - (R_C / r_e)$$

Phase relation: - sign in A_V indicates phase shift of 180° between input and output.

Collector DC feedback configuration



r_e model



$Z_i = R_{F1} \| \beta r_e$

Z_o =

$R_C \| R_{F2} \| r_o$, for $r_o \geq 10R_C$, $Z_o = R_C \| R_{F2}$

To find Voltage Gain A_V :

$$V_o = - \beta I_b (R_{F2} \| R_C \| r_o),\ I_b = V_i / \beta r_e$$

$$V_o = - \beta\ (V_i / \beta r_e)(R_{F2} \| R_C \| r_o)$$

$$V_o / V_i = - (R_{F2} \| R_C \| r_o) / r_e,$$

for $r_o \geq 10R_C$,

$$A_V = V_o / V_i = - (R_{F2} \| R_C) / r_e$$

Determining the current gain

For each transistor configuration, the current gain can be determined directly from the voltage gain, the defined load, and the input impedance.

We know that, current gain $(A_i) = I_o / I_i$

$$I_o = (V_o / R_L) \text{ and } I_i = V_i / Z_i$$

Thus,

$$A_i = - (V_o / R_L) / (V_i / Z_i)$$

$$= - (V_o Z_i / V_i R_L)$$

$$A_i = - A_V Z_i / R_L$$

Example:

For a voltage divider network, we have found that, $Z_i = \beta r_e$

$$A_V = - R_C / r_e \text{ and } R_L = R_C$$

Thus,

$$A_i = - A_V Z_i / R_L$$

$$= - (- R_C / r_e)(\beta r_e) / R_C$$

$$A_i = \beta$$

For a Common Base amplifier, $Z_i = r_e$, $A_V = R_C / r_e$, $R_L = R_C$

$$A_i = - A_V Z_i / R_L$$
$$= - (R_C / r_e)(r_e) / R_C$$
$$= - 1$$

Effect of R_L and R_S:

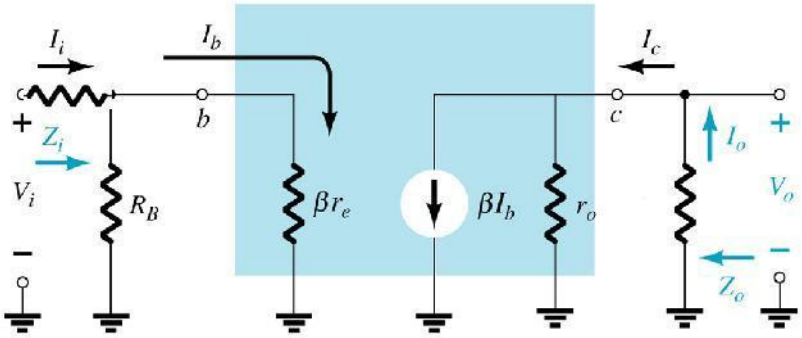
Voltage gain of an amplifier without considering load resistance (R_L) and source resistance (R_S) is A_{VNL}.

Voltage gain considering load resistance (R_L) is $A_V < A_{VNL}$ Voltage gain considering R_L and R_S is A_{VS}, where $A_{VS} < A_{VNL} < A_V$

For a particular design, the larger the level of R_L, the greater is the level of ac gain.

Also, for a particular amplifier, the smaller the internal resistance of the signal source, the greater is the overall gain.

Fixed bias with R_S and R_L:



$$A_V = - (R_C || R_L) / r_e$$

$$Z_i = R_B || \beta r_e$$

$$Z_o = R_C || r_o$$

To find the gain A_{VS}, (Z_i and R_S are in series and applying voltage divider rule)

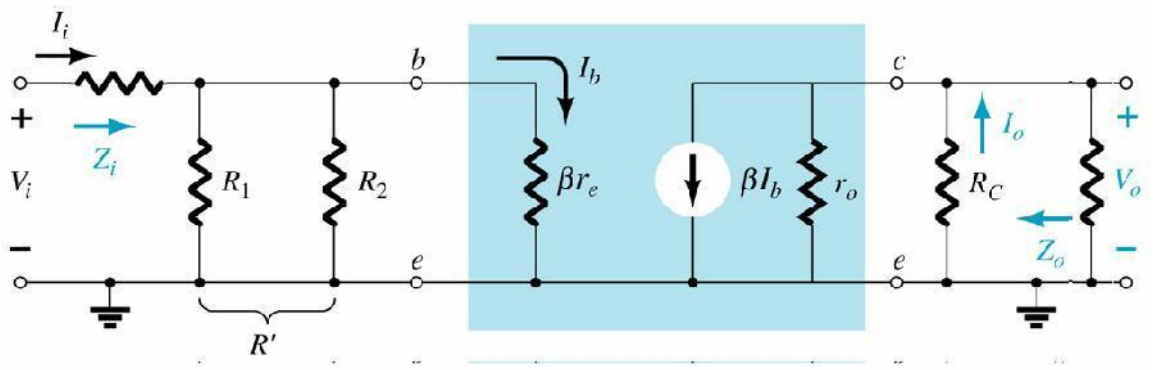
$$V_i = V_S Z_i / (Z_i + R_S)$$

$$V_i / V_S = Z_i / (Z_i + R_S)$$

$$A_{VS} = V_o / V_S = (V_o / V_i) (V_i / V_S)$$

$$A_{VS} = A_V [Z_i / (Z_i + R_S)]$$

Voltage divider with R_S and R_L

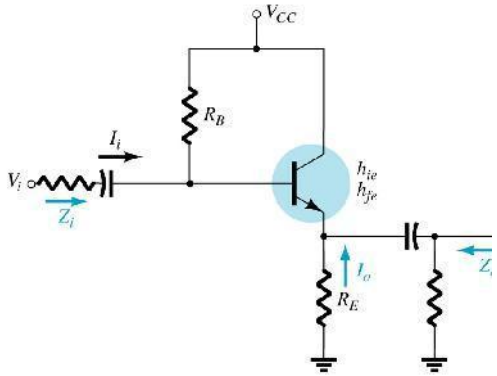


Voltage gain: $A_V = - [R_C||R_L] / r_e$

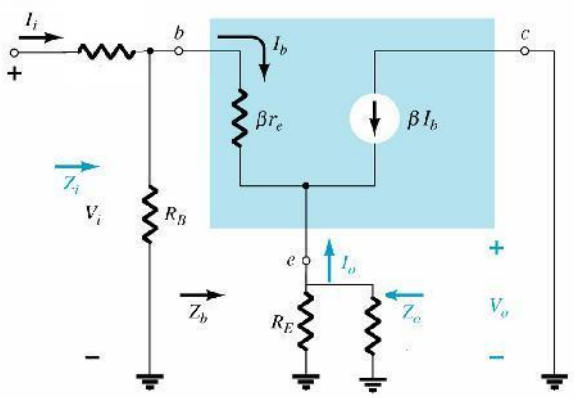
Input Impedance: $Z_i = R_1||R_2||\beta\ r_e$

Output Impedance: $Z_o = R_C||R_L||r_o$

Emitter follower with R_S and R_L



r_e model:



Voltage Gain: $A_V = (R_E||R_L) / [R_E||R_L+r_e]$

Input Impedance: $Z_i = R_B \,||\, Z_b$

Input Impedance seen at Base: $Z_b = \beta(R_E||R_L)$

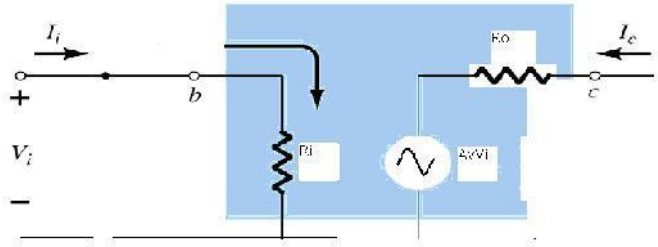
Output Impedance $Z_o = r_e$

Two – port systems approach

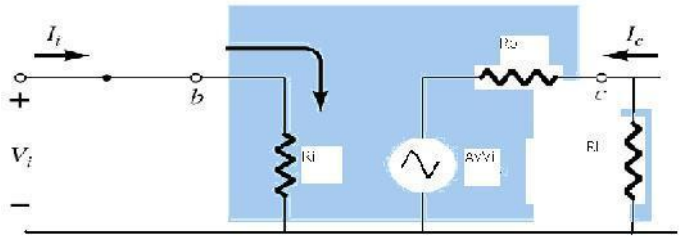
This is an alternative approach to the analysis of an amplifier.
This is important where the designer works with packaged with packaged products rather than individual elements.
An amplifier may be housed in a package along with the values of gain, input and output impedances.
But those values are no load values and by using these values, it is required to find out the gain and various impedances under loaded conditions.
This analysis assumes the output port of the amplifier to be seen as a voltage source. The value of this output voltage is obtained by Thevinising the output port of the amplifier.

$$E_{th} = A_{VNL}V_i$$

Model of two port system



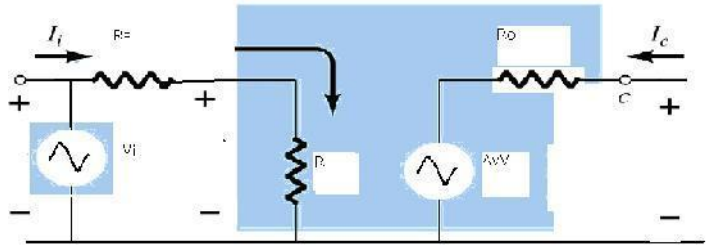
Applying the load to the two port system



Applying voltage divider in the above system:

$$V_o = A_{VNL}V_iR_L / [\, R_L+R_o]$$

Including the effects of source resistance R_S



Applying voltage divider at the input side, we get:

$$V_i = V_S R_i /[R_S+R_i]$$

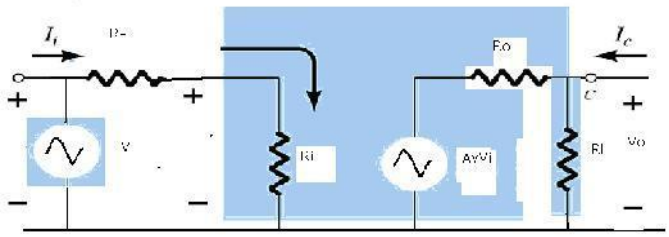
$$V_o = A_{VNL} V_i$$

$$V_i = V_S R_i /[R_S+R_i]$$

$$V_o = A_{VNL}\ V_S R_i /[R_S+R_i]$$

$$V_o/ V_S = A_{VS} = A_{VNL} R_i /[R_S+R_i]$$

Two port system with R_S and R_L



We know that, at the input side

$$V_i = V_S R_i /[R_S+R_i]$$

$$V_i / V_S = R_i /[R_S+R_i]$$

At the output side,

$$V_o = A_{VNL} V_i R_L / [\ R_L+R_o]$$

$$V_o / V_i = A_{VNL} R_L / [\ R_L+R_o]$$

Thus, considering both R_S and R_L:

$$A_V = V_o / V_s$$

$$= [V_o / V_i]\ [V_i / V_s]$$

$$A_V = (A_{VNL}R_L / [R_L+R_o]) (R_i / [R_S+R_i])$$

Example:

Given an amplifier with the following details:

$R_S = 0.2\ k\Omega$, $A_{VNL} = -480$, $Z_i = 4\ k\Omega$, $Z_o = 2\ k\Omega$

Determine:

A_V with $R_L = 1.2k\Omega$

A_V and A_i with $R_L = 5.6\ k\Omega$, A_{VS} with $R_L = 1.2$

Solution:

$A_V = A_{VNL}R_L / (R_L + R_o)$

$= (-480)1.2k / (1.2k+2k)$

$= -180$

With $R_L = 5.6k$, $A_V = -353.76$

This shows that, larger the value of load resistor, the better is the gain.

$A_{VS} = [R_i /(R_i+R_S)] [R_L / (R_L+R_o)] A_{VNL}$

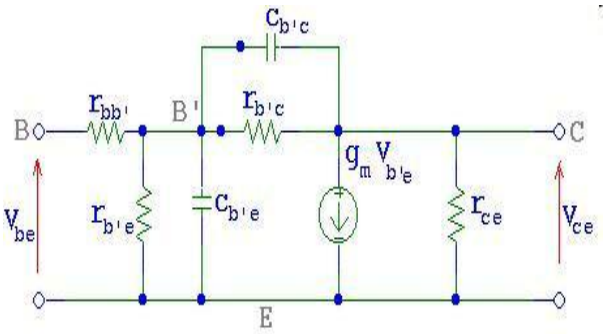
$= -171.36$

$A_i = -A_V Z_i/R_L$, here A_V is the voltage gain when $R_L = 5.6k$.

$A_i = -A_V Z_i/R_L$

$= -(-353.76)(4k/5.6k) = 252.6$

Hybrid π model



This is more accurate model for high frequency effects. The capacitors that appear are stray parasitic capacitors between the various junctions of the device. These capacitances come into picture only at high frequencies.

- C_{bc} or C_u is usually few pico farads to few tens of pico farads.
- r_{bb} includes the base contact, base bulk and base spreading resistances.

- r_{be} (r_π), r_{bc}, r_{ce} are the resistances between the indicated terminals.
- r_{be} (r_π) is simply βr_e introduced for the CE r_e model.
- r_{bc} is a large resistance that provides feedback between the output and the input.
- $r_\pi = \beta r_e$
- $g_m = 1/r_e$
- $r_o = 1/h_{oe}$
- $h_{re} = r$

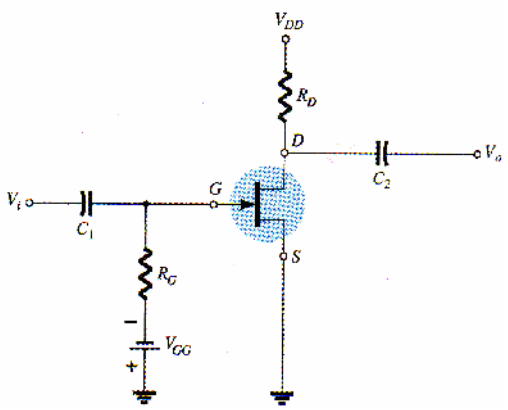
MODULE-II ,III

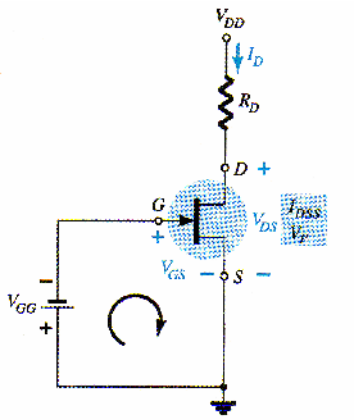
FET DC Biasing

The general relationships that can be applied to the dc analysis of all FET amplifiers

$$I_G \cong 0\ \text{A}$$

$$I_D = I_S$$





JFET & D-MOSFET, Shockley's equation is applied to relate the input & output quantities:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

For enhancement-type MOSFETs, the following equation is applicable:

$$I_D = k(V_{GS} - V_T)^2$$

Fixed-Bias Configuration

Since V_{GG} is a fixed dc supply, V_{GS} is fixed in magnitude

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

The fixed level of V_{GS} has been superimposed as a vertical line at ***$V_{GS} = -V_{GG}$****. **I_D** determined at any point on the vertical line (**V_{GS}** is **$-V_{GG}$**).*

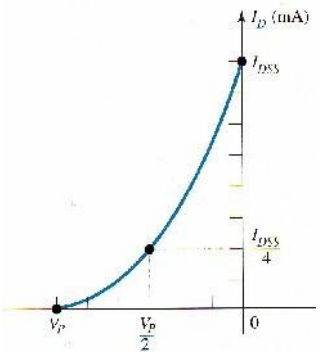


Fig-plotting Shockely's equation

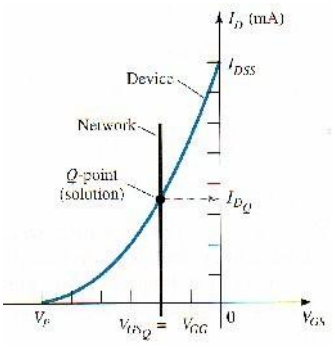
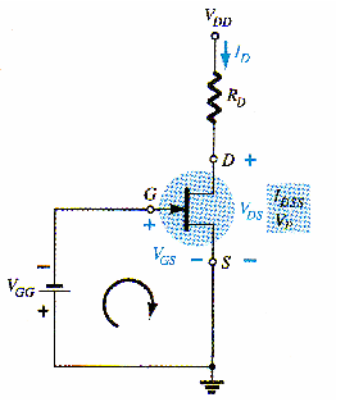


Fig-solution for the fixed bias configuration



$$+V_{DS} + I_D R_D - V_{DD} = 0$$

$$V_{DS} = V_{DD} - I_D R_D$$

$$V_S = 0\ \text{V}$$

$$V_{DS} = V_D - V_S$$

$$V_D = V_{DS} + V_S = V_{DS} + 0\ \text{V}$$

$$V_D = V_{DS}$$

In addition, $V_{GS} = V_G - V_S$

or $V_G = V_{GS} + V_S = V_{GS} + 0\ \text{V}$

and $V_G = V_{GS}$

Example1: *Determine the following for the network of (a) V_{GSQ} (b) I_{DQ} (c) V_{DS} (d) V_D (e) V_G (f) V_S*

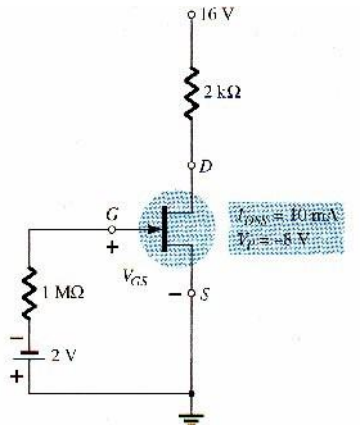


Fig- Example 1:

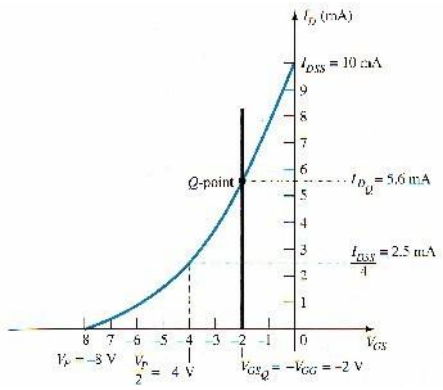


Fig-Graphical solution for Ex:1

Solution:

From the graph of fig8 -6 , 5.6mA is quite acceptable. Therefore, for part (a)

$$V_{GS_Q} = -V_{GG} = \mathbf{-2\ V}$$

(b) $I_{D_Q} = \mathbf{5.6\ mA}$

(c) $V_{DS} = V_{DD} - I_D R_D = 16\ \text{V} - (5.6\ \text{mA})(2\ \text{k}\Omega)$

$= 16\ \text{V} - 11.2\ \text{V} = \mathbf{4.8\ V}$

(d) $V_D = V_{DS} = \mathbf{4.8\ V}$

(e) $V_G = V_{GS} = \mathbf{-2\ V}$

(f) $V_S = \mathbf{0\ V}$

Self-Bias Configuration

The controlling gate-to-source voltage is now determined by the voltage across a resistor $\boldsymbol{R_S}$ *introduced in the source leg of the configuration in fig*

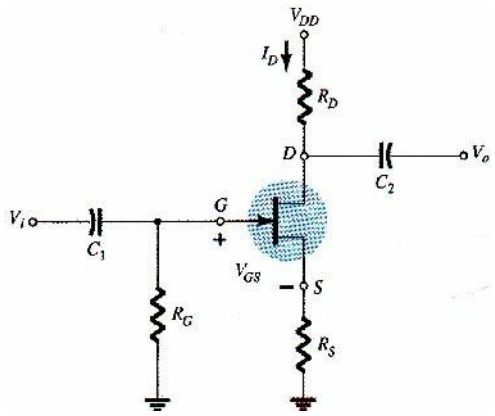


Fig- JFET self-bias configuration

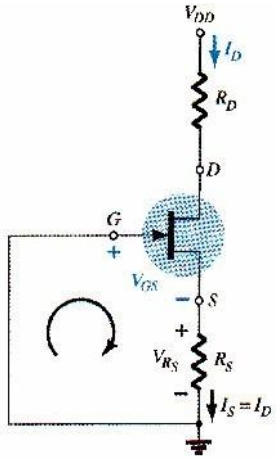


Fig-DC analysis of the self configuration

The current through R_S is the source current ***I_S*** *but* ***$I_S = I_D$*** *and*

$$V_{R_S} = I_D R_S$$

For the indicated closed loop of fig 8-8 we find that

$$-V_{GS} - V_{R_S} = 0$$

and $$V_{GS} = -V_{R_S}$$

or $$V_{GS} = -I_D R_S$$

Substituting this equation into Shockley"s equation as below:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(1 - \frac{-I_D R_S}{V_P}\right)^2$$

$$I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

so we must identify two point , ***the first*** *point as defines shown .* ***The second*** *point identifies by using this approximating:*

Then $$V_{GS} = -I_D R_S = -\frac{I_{DSS} R_S}{2}$$

$$I_D = \frac{I_{DSS}}{2}$$

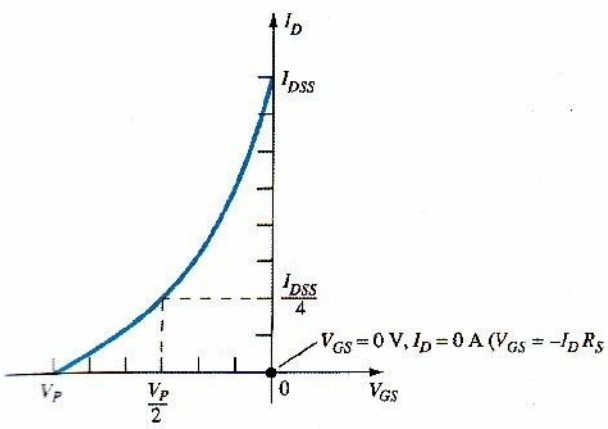


Fig-defining a point on the self-bias line

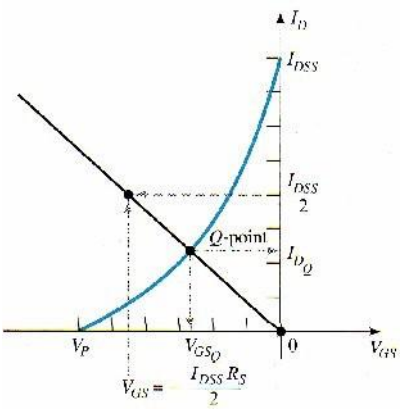


Fig- sketching the self-bias line

Applying KVL to the output circuit to determine the V_{DS}

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

and $$V_{DS} = V_{DD} - V_{R_S} - V_{R_D} = V_{DD} - I_S R_S - I_D R_D$$

but $I_D = I_S$

and $V_{DS} = V_{DD} - I_D(R_S + R_D)$

$V_S = I_D R_S$

$V_G = 0\ \text{V}$

and $V_D = V_{DS} + V_S = V_{DD} - V_{R_D}$

Example 2: *Determine the following for the network of fig8-11,(a) V_{GSQ} (b) I_{DQ} (c) V_{DS} (d) V_S (e) V_G (f) V_D*

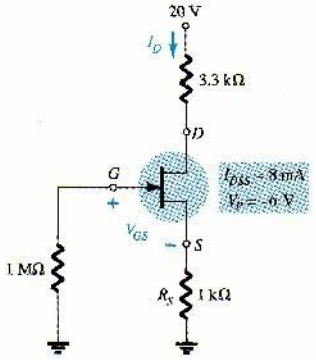


Fig- Example2:

Solution:

$$V_{GS} = -I_D R_S$$

Choosing ***I_D = 4mA****, we obtain*

$$V_{GS} = -(4\ \text{mA})(1\ \text{k}\Omega) = -4\ \text{V}$$

The result is the plot of fig8-12 as defined by the network, If choose $V_{GS} = V_P / 2 = -3V$, we find

$I_D = I_{DSS}/4 = 8mA / 4 = 2mA$, *as shown in fig 8-13*

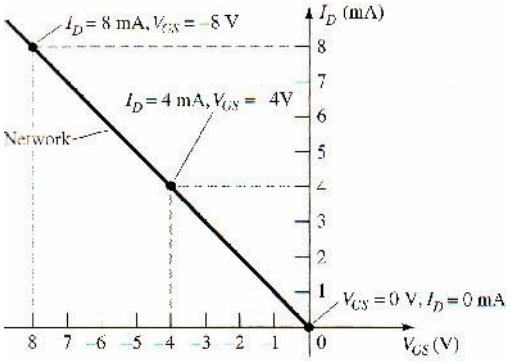


Fig-self bias line for Ex2:

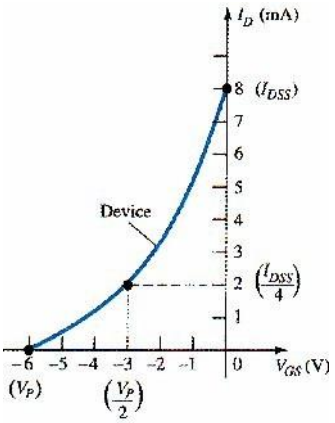


Fig- JFET of Ex2

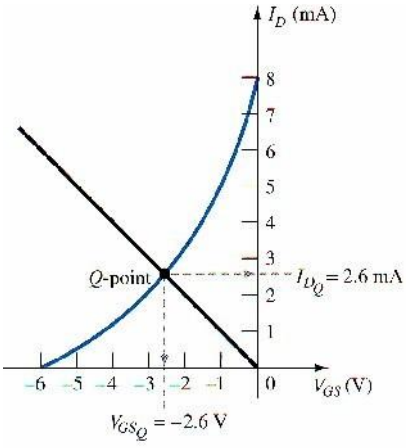


Fig- Q-point for the network

$$V_{GS_Q} = -2.6 \text{ V}$$

(b) At the quiescent point:

$$I_{D_Q} = 2.6 \text{ mA}$$

(c)

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$
$$= 20\text{ V} - (2.6\text{ mA})(1\text{ k}\Omega + 3.3\text{ k}\Omega)$$
$$= 20\text{ V} - 11.18\text{ V}$$
$$= \mathbf{8.82\text{ V}}$$

(d)

$$= (2.6\text{ mA})(1\text{ k}\Omega)$$
$$= \mathbf{2.6\text{ V}}$$

(e)

$$V_G = \mathbf{0\text{ V}}$$

(f)

$$V_D = V_{DS} + V_S = 8.82\text{ V} + 2.6\text{ V} = \mathbf{11.42\text{ V}}$$
$$V_D = V_{DD} - I_D R_D = 20\text{ V} - (2.6\text{ mA})(3.3\text{ k}\Omega) = \mathbf{11.42\text{ V}}$$

Example3: *Find the quiescent point for the network of fig8-11 if(a) RS=100Ω, (b) RS=10kΩ*

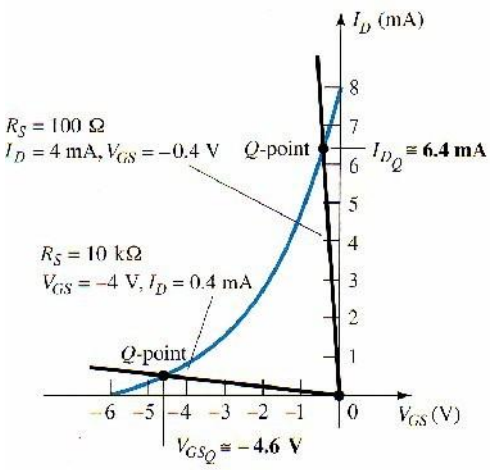


Fig-Example 3:

(a)I_D scale

$$I_{D_Q} \cong \mathbf{6.4\text{ mA}}$$

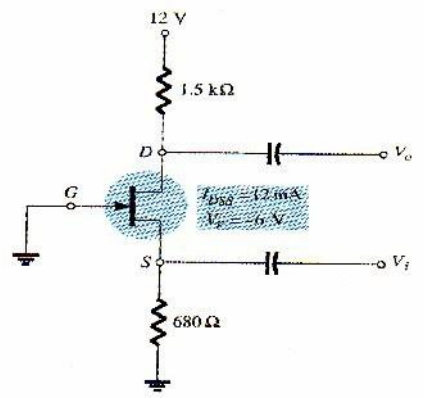
$$V_{GS_Q} \cong \mathbf{-0.64\text{ V}}$$

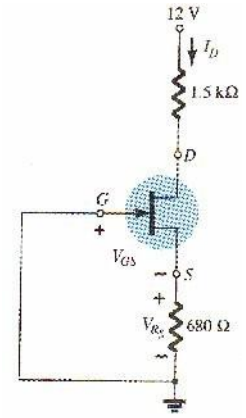
V_{GS} scale,

$$V_{GS_Q} \cong \mathbf{-4.6\text{ V}}$$

$$I_{D_Q} \cong \mathbf{0.46\ mA}$$

Example4: *Determine the following for the common-gate configuration of fig(a)V_{GSQ} (b) I_D (c) V_D (d)V_G (e)V_S (f)V_{DS}*





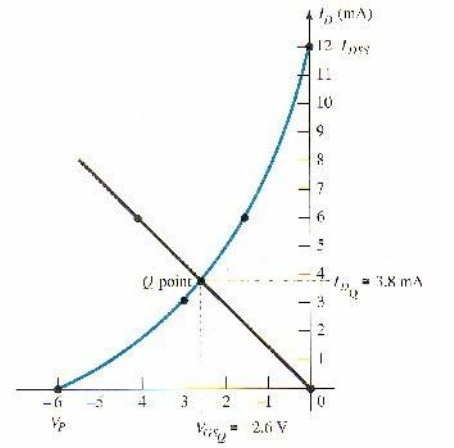


Fig-Example 4: *he dc resulting* *Fig - Q-point for the network*

Solution:

a) The transfer characteristic and load line appear in fig8-18. ***The second*** *point for the sketch of the load line was determined by choosing (arbitrarily)* I_D***=6mA,*** *solving for* V_{GS}

$$V_{GS} = -I_D R_S = -(6\text{ mA})(680\ \Omega) = -4.08\text{ V}$$

As shown in fig8-18. The device transfer curve was sketched using

$$I_D = \frac{I_{DSS}}{4} = \frac{12\text{ mA}}{4} = 3\text{ mA}$$

$$V_{GS} = \frac{V_P}{2} = -\frac{6\text{ V}}{2} = -3\text{ V}$$

The resulting quiescent point of fig is:

$$V_{GS_Q} \cong \mathbf{-2.6\text{ V}}$$

(b)

$$I_{D_Q} \cong \mathbf{3.8\text{ mA}}$$

(c) $V_D = V_{DD} - I_D R_D$

$= 12\text{ V} - (3.8\text{ mA})(1.5\text{ k}\Omega) = 12\text{ V} - 5.7\text{ V}$

$= \mathbf{6.3\text{ V}}$

(d) $V_G = \mathbf{0\text{ V}}$

(e) $V_S = I_D R_S = (3.8\text{ mA})(680\ \Omega)$

$= \mathbf{2.58\text{ V}}$

(f) $V_{DS} = V_D - V_S$

$= 6.3\text{ V} - 2.58\text{ V}$

$= \mathbf{3.72\text{ V}}$

Voltage-Divider Biasing

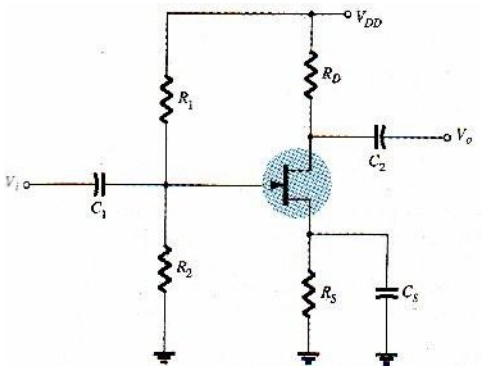


Fig- voltage-divider bias arrangement

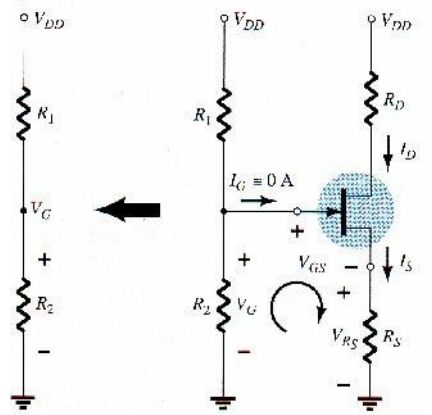


Fig-redrawn network for dc analysis

***I_G = 0 A**, KCL requires that **I_{R1} = I_{R2}**, V_G found using Voltage Divider Rule as:*

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Applying KVL in the clockwise direction to the indicated loop of fig

$$V_G - V_{GS} - V_{R_S} = 0$$

$$V_{GS} = V_G - V_{R_S}$$

$V_{R_S} = I_S R_S = I_D R_S$, we have

$$V_{GS} = V_G - I_D R_S$$

Set I_D = 0mA resulting:

$$V_{GS} = V_G - I_D R_S$$
$$= V_G - (0\,\text{mA})R_S$$

$$V_{GS} = V_G|_{I_D = 0\,\text{mA}}$$

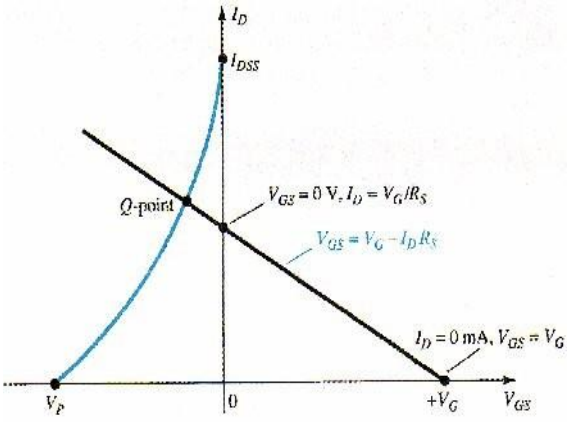


Fig-the network equation

For the other point, let us now employ the fact that:

$$V_{GS} = V_G - I_D R_S$$
$$0\,\text{V} = V_G - I_D R_S$$

$$I_D = \frac{V_G}{R_S}\bigg|_{V_{GS} = 0\,\text{V}}$$

Increasing values of R_S result in lower quiescent values of I_D and more negative values of V_{GS}

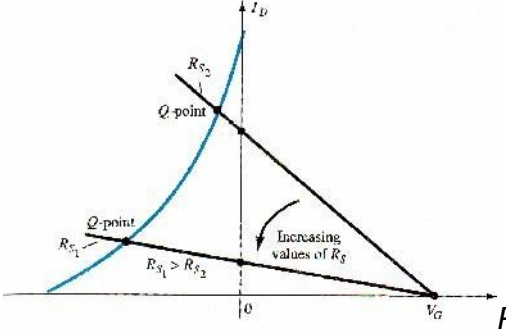


Fig-effect of R_S on the resulting Q-point

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

$$V_D = V_{DD} - I_D R_D$$

$$V_S = I_D R_S$$

$$I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2}$$

Example 5: *Determine the following for the network of fig,(a) I_{DQ} & V_{GSQ} (b) V_D (c) V_S (d) V_{DS} (e) V_{DG}*

Solution*: a) For the transfer char-, if $I_D=I_{DSS}/4$ =8mA/4=2mA, then $V_{GS}=V_P/2$=-4V/2 =-2V*
The resulting curve in fig; the network equation is defined by:

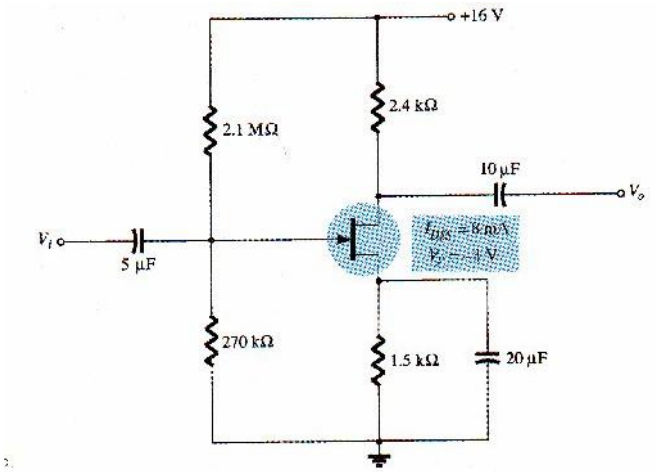


Fig-Example 5:

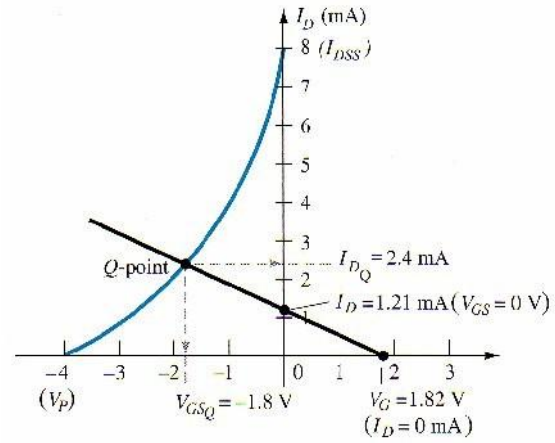


*Fig-the **Q**-point for the network*

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$= \frac{(270\ \text{k}\Omega)(16\ \text{V})}{2.1\ \text{M}\Omega + 0.27\ \text{M}\Omega}$$

$$= 1.82\ \text{V}$$

$$V_{GS} = V_G - I_D R_S$$

$$= 1.82\ \text{V} - I_D(1.5\ \text{k}\Omega)$$

When $I_D = 0$ mA:

$$V_{GS} = +1.82\ \text{V}$$

When $V_{GS} = 0$ V:

$$I_D = \frac{1.82\ \text{V}}{1.5\ \text{k}\Omega} = 1.21\ \text{mA}$$

The resulting bias line appears on fig with quiescent values of

$$I_{D_Q} = 2.4\ \text{mA}$$

and $$V_{GS_Q} = -1.8\ \text{V}$$

(b) $$V_D = V_{DD} - I_D R_D$$

$$= 16\ \text{V} - (2.4\ \text{mA})(2.4\ \text{k}\Omega)$$

$$= 10.24\ \text{V}$$

(c) $$V_S = I_D R_S = (2.4\ \text{mA})(1.5\ \text{k}\Omega)$$

$$= 3.6\ \text{V}$$

(d) $$V_{DS} = V_{DD} - I_D(R_D - R_S)$$

$$= 16\ \text{V} - (2.4\ \text{mA})(2.4\ \text{k}\Omega + 1.5\ \text{k}\Omega)$$

$$= 6.64\ \text{V}$$

or $$V_{DS} = V_D - V_S = 10.24\ \text{V} - 3.6\ \text{V}$$

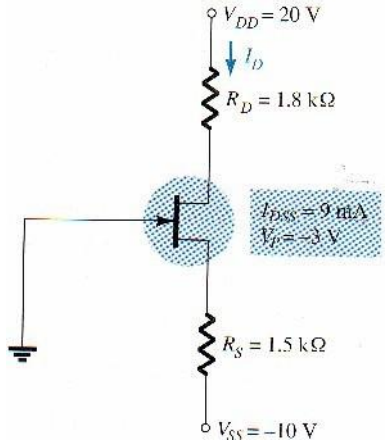
$$= 6.64\ \text{V}$$

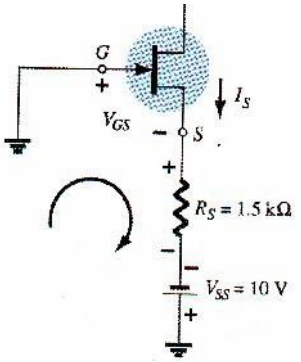
$$V_{DG} = V_D - V_G$$

$$= 10.24\ \text{V} - 1.82\ \text{V}$$

$$= 8.42\ \text{V}$$

Example6: *Determine the following for the network of fig8-25, ,(a) I_{DQ} & V_{GSQ} (b) V_{DS} (c) V_D (d) V_S*





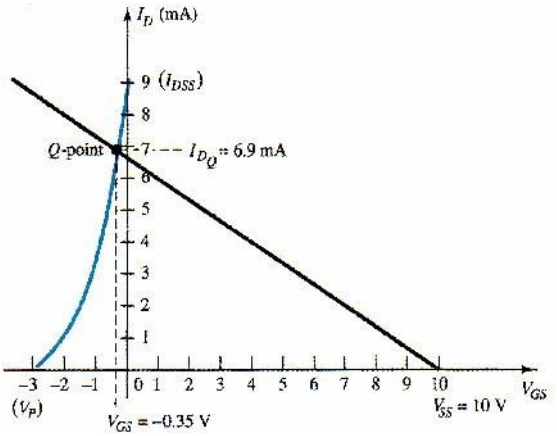


Fig-Ex6 *Fig-the network* *Fig-Q-point*

Solution:

a) Applying KVL to the input section of the network redrawn in fig 8-26

$$-V_{GS} - I_S R_S + V_{SS} = 0$$

or $$V_{GS} = V_{SS} - I_S R_S$$

but $$I_S = I_D$$

and $$\boxed{V_{GS} = V_{SS} - I_D R_S}$$

$$V_{GS} = 10\text{ V} - I_D(1.5\text{ k}\Omega)$$

For $I_D = 0$ mA,

$$V_{GS} = V_{SS} = 10\text{ V}$$

For $V_{GS} = 0$ V,

$$0 = 10\text{ V} - I_D(1.5\text{ k}\Omega)$$

and $$I_D = \frac{10\text{ V}}{1.5\text{ k}\Omega} = 6.67\text{ mA}$$

For the transfer char-, $V_{GS}=V_P/2=-3V/2 =-1.5V$ and $I_D=I_{DSS}/4 =9mA/4=2.25mA$

$$I_{D_Q} = \mathbf{6.9\text{ mA}}$$

$$V_{GS_Q} = \mathbf{-0.35\text{ V}}$$

b) Applying KVL to the output side of fig will result

$$-V_{SS} + I_S R_S + V_{DS} + I_D R_D - V_{DD} = 0$$

Substituting $I_S = I_D$ and rearranging gives

$$V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)$$

$$V_{DS} = 20\text{ V} + 10\text{ V} - (6.9\text{ mA})(1.8\text{ k}\Omega + 1.5\text{ k}\Omega)$$

$$= 30\text{ V} - 22.77\text{ V}$$

$$= \mathbf{7.23\text{ V}}$$

(c) $V_D = V_{DD} - I_D R_D$

$$= 20\text{ V} - (6.9\text{ mA})(1.8\text{ k}\Omega) = 20\text{ V} - 12.42\text{ V}$$

$$= \mathbf{7.58\text{ V}}$$

(d) $V_{DS} = V_D - V_S$

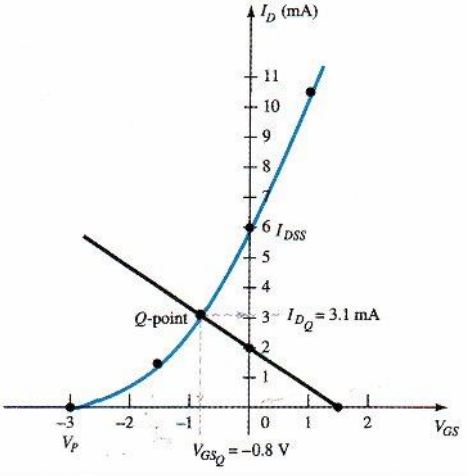
or $V_S = V_D - V_{DS}$

$$= 7.58\text{ V} - 7.23\text{ V}$$

$$= \mathbf{0.35\text{ V}}$$

Depletion –Type MOSFETS

Example 7: *For the n-channel depletion-type of fig , determine: I_{DQ} & V_{GSQ} & V_{DS}*



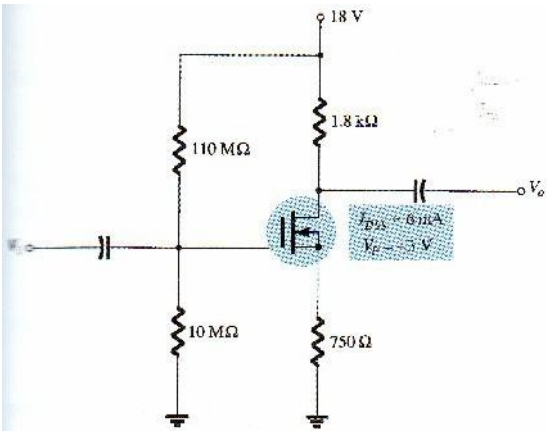


Fig-n-DMOSFET Example 7: *Fig-Q-point for the network of Ex7n-DMOSFET*

Setting $I_D = 0$ mA results in

$$V_{GS} = V_G = 1.5 \text{ V}$$

Setting $V_{GS} = 0$ V yields

$$I_D = \frac{V_G}{R_S} = \frac{1.5 \text{ V}}{750\ \Omega} = 2 \text{ mA}$$

Solution: *For the transfer char-, $V_{GS}=V_P/2=-3V/2 =-1.5V$ and $I_D=I_{DSS}/4 =6mA/4=1.5mA$, consider the level of V_P and the fact that Skockley's equation defines a curve that rises more positive. A plot point will defined at $V_{GS} =+1V$.*

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
$$= 6\text{ mA}\left(1 - \frac{+1\text{ V}}{-3\text{ V}}\right)^2 = 6\text{ mA}\left(1 + \frac{1}{3}\right)^2 = 6\text{ mA}(1.778)$$
$$= 10.67\text{ mA}$$

Eq[8-15]

$$V_G = \frac{10\text{ M}\Omega(18\text{ V})}{10\text{ M}\Omega + 110\text{ M}\Omega} = 1.5\text{ V}$$

Eq[8-16]

$$V_{GS} = V_G - I_D R_S = 1.5\text{ V} - I_D(750\ \Omega)$$

The plot point and resulting bias line appear in fig8-29 the resulting operating point:

b)Eq[8-19]

$$I_{D_Q} = \mathbf{3.1\text{ mA}}$$
$$V_{GS_Q} = \mathbf{-0.8\text{ V}}$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$
$$= 18\text{ V} - (3.1\text{ mA})(1.8\text{ k}\Omega + 750\ \Omega)$$
$$\cong \mathbf{10.1\text{ V}}$$

Example 8: *Repeat Example 7: with R_S = 150Ω*

Solution: *(a) The plot points are the same for the transfer curve as shown in fig8-30,*

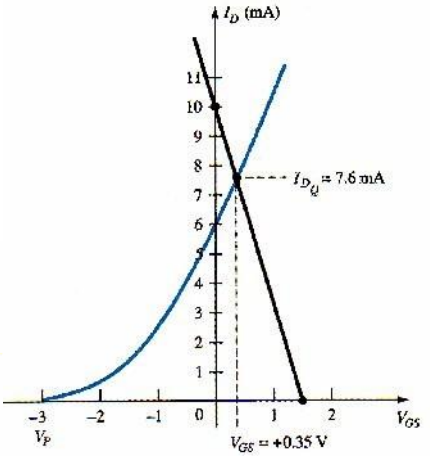
$$V_{GS} = V_G - I_D R_S = 1.5\text{ V} - I_D(150\ \Omega)$$

Setting $I_D = 0$ mA results in

$$V_{GS} = 1.5 \text{ V}$$

Setting $V_{GS} = 0$ V yields

$$I_D = \frac{V_G}{R_S} = \frac{1.5 \text{ V}}{150\ \Omega} = 10 \text{ mA}$$



$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$
$$= 18 \text{ V} - (7.6 \text{ mA})(1.8 \text{ k}\Omega + 150\ \Omega)$$

Example 9: *Determine the following for the network of fig-, I_{DQ} & V_{GSQ} & V_D*

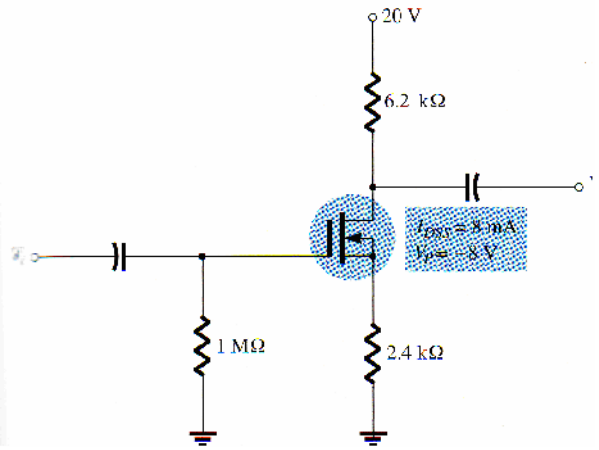


Fig-Example 9:

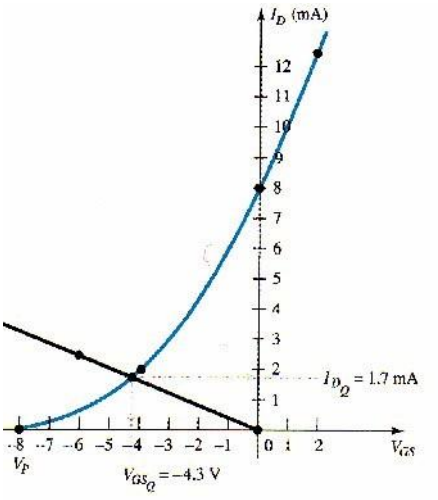


Fig-the Q-point for the network of Ex9:

Solution:

$$V_{GS} = -I_D R_S$$

For JFET V_{GS} must be less than zero volts. Therefore no requirement to plot the transfer curves for positive values of V_{GS}

$$I_D = \frac{I_{DSS}}{4} = \frac{8 \text{ mA}}{4} = 2 \text{ mA}$$

and

$$V_{GS} = \frac{V_P}{2} = \frac{-8 \text{ V}}{2} = -4 \text{ V}$$

and for $V_{GS} > 0$ V, since $V_P = -8$ V, we will choose

$$V_{GS} = +2 \text{ V}$$

For the network bias line, at V_{GS}=0V, I_D=0mA. Choosing V_{GS} = -6V

$$I_D = -\frac{V_{GS}}{R_S} = -\frac{-6\text{ V}}{2.4\text{ k}\Omega} = 2.5\text{ mA}$$

The resulting Q-point:

$$I_{D_Q} = \mathbf{1.7\text{ mA}}$$

$$V_{GS_Q} = \mathbf{-4.3\text{ V}}$$

(b) $V_D = V_{DD} - I_D R_D$

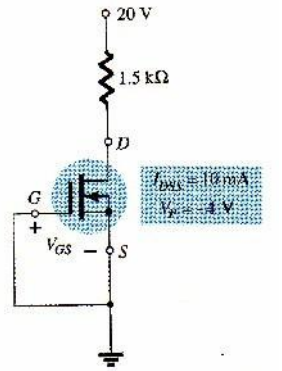
$= 20\text{ V} - (1.7\text{ mA})(6.2\text{ k}\Omega)$

$= \mathbf{9.46\text{ V}}$

Example 10: *Determine V_{DS} for the network of fig8-33*

Solution:

$$V_{GS} = 0 \text{ V}$$



$$V_{GS_Q} = \mathbf{0\ V}$$

$$I_{D_Q} = \mathbf{10\ mA}$$

$$V_D = V_{DD} - I_D R_D = 20 \text{ V} - (10 \text{ mA})(1.5 \text{ k}\Omega)$$
$$= 20 \text{ V} - 15 \text{ V}$$

Fig-Example10:

Enhancement-Type MOSFETs

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$

$$I_{D(\text{on})} = k(V_{GS(\text{on})} - V_{GS(\text{Th})})^2$$

$$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$$

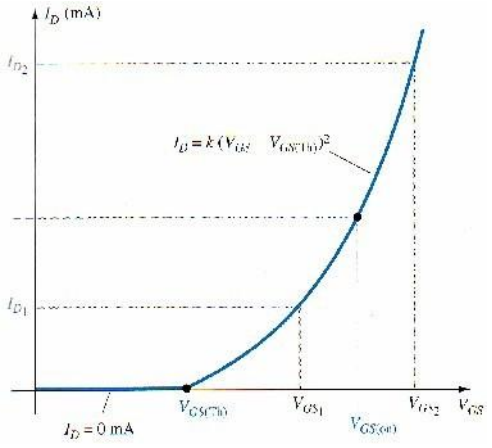


Fig-Transfer char- of n-EMOSFET

Feedback Biasing Arrangement

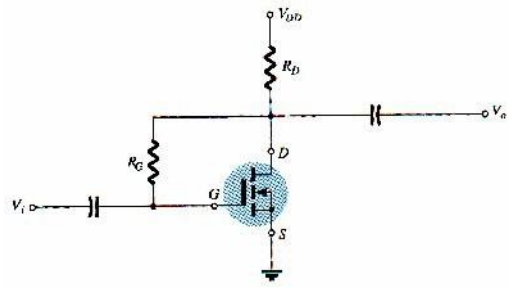


Fig-Feedback biasing arrangement

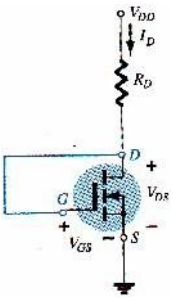


Fig-Dc equivalent of the network

A direct connection now exists between drain and gate, resulting in

$$V_D = V_G$$

and

$$V_{DS} = V_{GS}$$

For the output circuit,

$$V_{DS} = V_{DD} - I_D R_D$$

Which becomes the following after substituting

$$V_{GS} = V_{DD} - I_D R_D$$

Substituting I_D = 0mA

$$V_{GS} = V_{DD}|_{I_D = 0\,\text{mA}}$$

Substituting V_{GS} = 0mA

$$I_D = \frac{V_{DD}}{R_D}\bigg|_{V_{GS} = 0\,\text{V}}$$

the resulting operation point

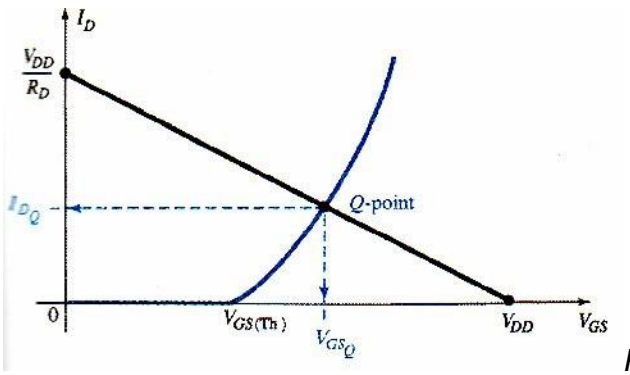


Fig-Q-point for the network

Example 11: *Determine I_{DQ} and V_{DSQ} for the enhancement-type MOSFET*

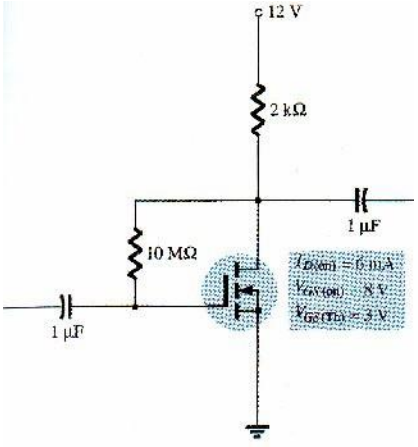


Fig-Example 11:

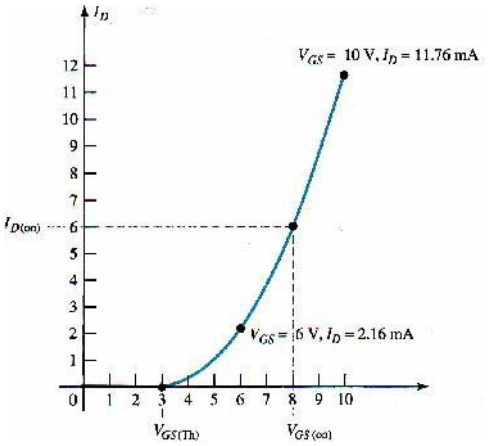


Fig-transfer curve for the MOSFET of Ex 11

Solution: *Two points are defined immediately as shown in fig. Solving for k*

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}$$

$$= \frac{6\text{ mA}}{(8\text{ V} - 3\text{ V})^2} = \frac{6 \times 10^{-3}}{25}\text{ A/V}^2$$

$$= \mathbf{0.24 \times 10^{-3}\text{ A/V}^2}$$

For V_{GS} = 6 V (between 3 and 8 V):

$$I_D = 0.24 \times 10^{-3}(6\text{ V} - 3\text{ V})^2 = 0.24 \times 10^{-3}(9)$$

$$= 2.16\text{ mA}$$

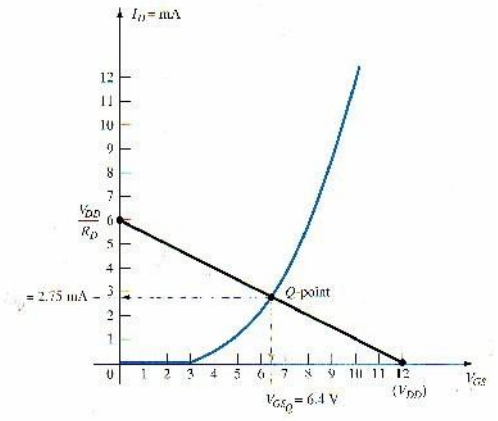
For V_{GS} = 10 V (slightly greater than $V_{GS(Th)}$):

$$I_D = 0.24 \times 10^{-3}(10\text{ V} - 3\text{ V})^2 = 0.24 \times 10^{-3}(49)$$

$$= 11.76\text{ mA}$$

For the Network Bias Line:

$$V_{GS} = V_{DD} - I_D R_D$$
$$= 12\ \text{V} - I_D(2\ \text{k}\Omega)$$
$$V_{GS} = V_{DD} = 12\ \text{V}|_{I_D = 0\ \text{mA}}$$
$$I_D = \frac{V_{DD}}{R_D} = \frac{12\ \text{V}}{2\ \text{k}\Omega} = 6\ \text{mA}|_{V_{GS} = 0\ \text{V}}$$



$I_{D_Q} = \mathbf{2.75\ mA}$

$V_{GS_Q} = 6.4\ \text{V}$

$V_{DS_Q} = V_{GS_Q} = \mathbf{6.4\ V}$

Fig-Q-point for the network

Voltage-Divider Biasing Arrangement

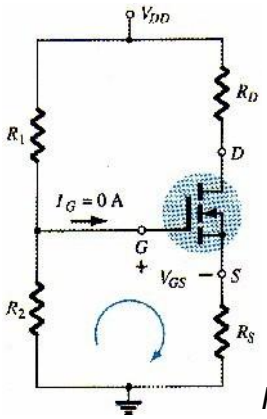


Fig8-41 Voltage-divider biasing for n- EMOSFET

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Applying KVL around the indicated loop of fig8-41 will result

$$+V_G - V_{GS} - V_{R_S} = 0$$

$$V_{GS} = V_G - V_{R_S}$$

$$V_{GS} = V_G - I_D R_S$$

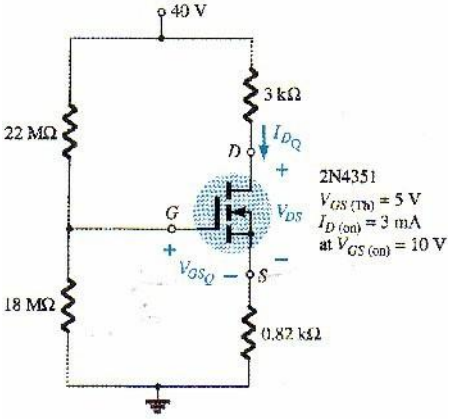
For the output section:

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D}$$

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

Example 12: *Determine I_{DQ} , V_{GSQ} , and V_{DS} for the network*



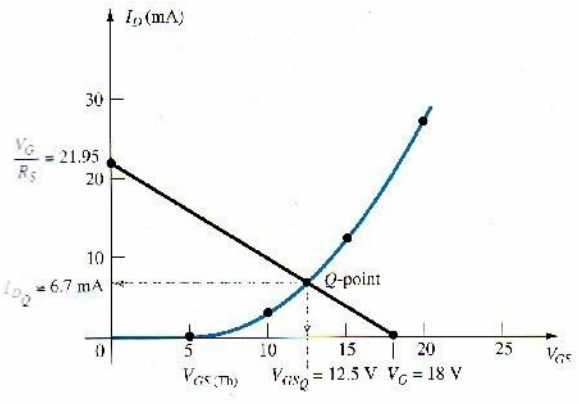


Fig-Example 12: *Fig-Q-point for network of Ex 12:*

Solution: Network:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(18\ \text{M}\Omega)(40\ \text{V})}{22\ \text{M}\Omega + 18\ \text{M}\Omega} = 18\ \text{V}$$

$$V_{GS} = V_G - I_D R_S = 18\ \text{V} - I_D(0.82\ \text{k}\Omega)$$

When I_D = 0mA

$$V_{GS} = 18\ \text{V} - (0\ \text{mA})(0.82\ \text{k}\Omega) = 18\ \text{V}$$

As appearing on fig 8-43, when V_{GS} = 0 V

$$V_{GS} = 18\ \text{V} - I_D(0.82\ \text{k}\Omega)$$

$$0 = 18\ \text{V} - I_D(0.82\ \text{k}\Omega)$$

$$I_D = \frac{18\ \text{V}}{0.82\ \text{k}\Omega} = 21.95\ \text{mA}$$

$$V_{GS(\text{Th})} = 5\ \text{V}, \qquad I_{D(\text{on})} = 3\ \text{mA with } V_{GS(\text{on})} = 10\ \text{V}$$

:

$$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$$

$$= \frac{3\ \text{mA}}{(10\ \text{V} - 5\ \text{V})^2} = 0.12 \times 10^{-3}\ \text{A/V}^2$$

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$

$$= 0.12 \times 10^{-3}(V_{GS} - 5)^2$$

$$I_{D_Q} \cong \mathbf{6.7\ mA}$$

$$V_{GS_Q} = \mathbf{12.5\ V}$$

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

$$= 40\ \text{V} - (6.7\ \text{mA})(0.82\ \text{k}\Omega + 3.0\ \text{k}\Omega)$$

$$= 40\ \text{V} - 25.6\ \text{V}$$

$$= \mathbf{14.4\ V}$$

SUMMARY

1- A fixed-bias configuration has, a fixed dc voltage applied from gate to source to establish the operating point.

2- The nonlinear relationship between the gate-to-source voltage and the drain current of a JFET requires that a graphical or mathematical solution be used to determine the quiescent point of operation.

3- All voltages with a single subscript define a voltage from a specified point to ground.

4- The self-bias configuration is determined by an equation for V_{GS} that will always pass through the origin. Any other point determined by the biasing equation will establish a straight line to represent the biasing network.

5- For the voltage-divider biasing configuration, one can always assume that the gate current is

0A to permit isolation or the voltage-divider network from the output section. The resulting gate-to-ground voltage will always be positive for an n-channel JFET and negative for a p-channel JFET. Increasing values of R_s result in lower quiescent values of I_D and more negative values of V_{GS} for an n-channel JFET

6- The method of analysis applied to depletion-type MOSFETs is the same as applied to

JFETs, with the only difference being a possible operating point with an I_D level above the I_{DSS}

value.

7- The characteristics and method of analysis applied to enhancement-type MOSFETs are entirely different from those of JFETs and depletion-type MOSFETs. For values of V_{GS} less than the threshold value, the drain current I_D is 0A.

8- When analyzing networks with a variety of devices. First work with the region of the network

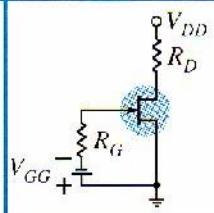
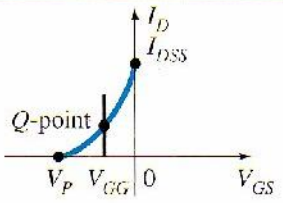
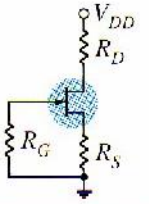
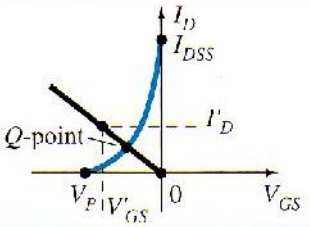
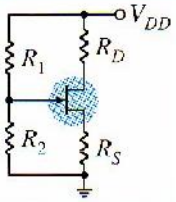
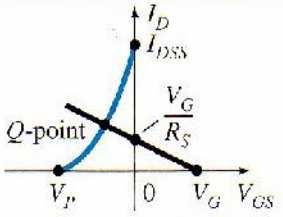
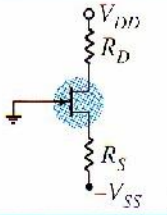
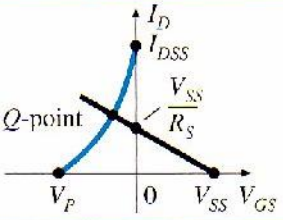
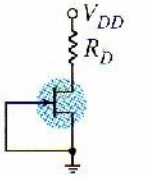
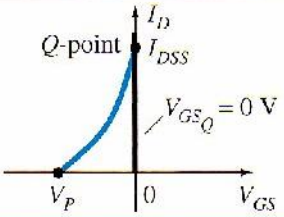
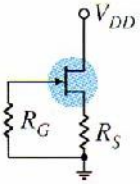
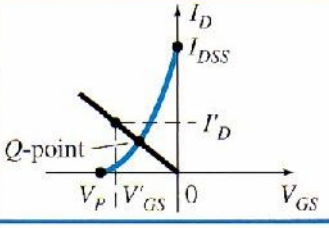
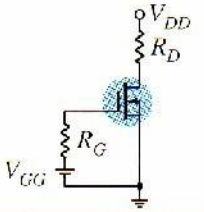
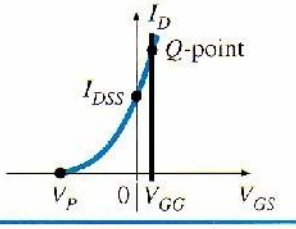
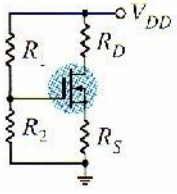
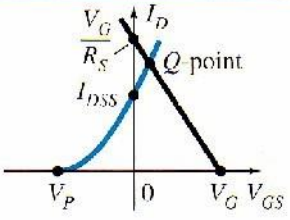
that will provide a voltage or current level using the basic relationships associated with those devices. Then use that level and the appropriate equations to find other voltage or current levels of the net work in the surrounding region of the system.

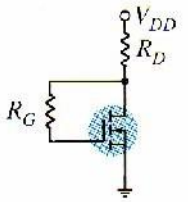
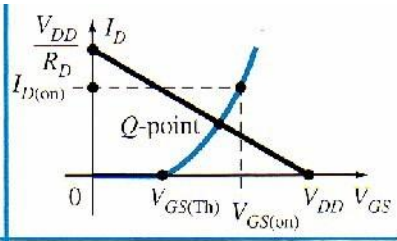
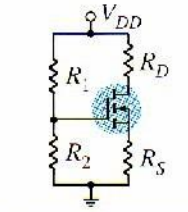
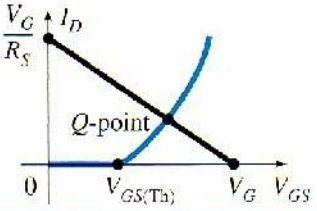
9- The design process often requires finding a resistance level to establish the desired voltage or current level. With this in mind remember that a resistance level is defined by the voltage

across the resistor divided by the current through the resistor. In the design process, both of these quantities are often available for a particular resistive element.

10- The analysis of p-channel FETs is the same as that applied to n-channel FETs except for the fact that all the voltages will have the opposite polarity and the currents the opposite direction

SUMMARY TABLE

Type	Configuration	Pertinent Equations	Graphical Solution
JFET Fixed-bias		$V_{GS_Q} = -V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
JFET Self-bias		$V_{GS} = -I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Voltage-divider bias		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Common-gate		$V_{GS} = V_{SS} - I_D R_S$ $V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)$	
JFET ($V_{GS_Q} = 0$ V)		$V_{GS_Q} = 0$ V $I_{D_Q} = I_{DSS}$	
JFET ($R_D = 0\ \Omega$)		$V_{GS} = -I_D R_S$ $V_D = V_{DD}$ $V_S = I_D R_S$ $V_{DS} = V_{DD} - I_S R_S$	
Depletion-type MOSFET Fixed-bias		$V_{GS_Q} = +V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
Depletion-type MOSFET Voltage-divider bias		$V_G = \frac{R_2 V_{DD}}{R_1 - R_2}$ $V_{GS} = V_G - I_S R_S$ $V_{DS} = V_{DD} - I_D(R_D - R_S)$	

Enhancement type MOSFET Feedback configuration		$V_{GS} = V_{DS}$ $V_{GS} = V_{DD} - I_D R_D$	
Enhancement type MOSFET Voltage-divider bias		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$	

Equations:

JFETs/depletion-type MOSFETs:

Fixed-bias configuration: $V_{GS} = -V_{GG} = V_G$

Self-bias configuration: $V_{GS} = -I_D R_S$

Voltage-divider biasing: $V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$

$V_{GS} = V_G - I_D R_S$

Enhancement-type MOSFETs:

Feedback biasing: $V_{DS} = V_{GS}$

$V_{GS} = V_{DD} - I_D R_D$

Voltage-divider biasing: $V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$

$V_{GS} = V_G - I_D R_S$

MODULE-III

FET Small signal analysis

The gate-to-source ac voltage controls the drain-to-source (channel) current of an FET, Skockley's equation controlled the level of dc drain current through a relationship

$$\Delta I_D = g_m \Delta V_{GS} \left(\frac{V_{GS}}{V_P} \right)^2$$

***g_m** is a trans-conductance factor using to determined The change in Drain current that will result from a change in gate-to-source voltage in the following:*

Conductance of resistor g = 1/R = I/V

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

Graphical Determination of g_m

$$g_m = m = \frac{\Delta y}{\Delta x} = \frac{\Delta I_D}{\Delta V_{GS}}$$

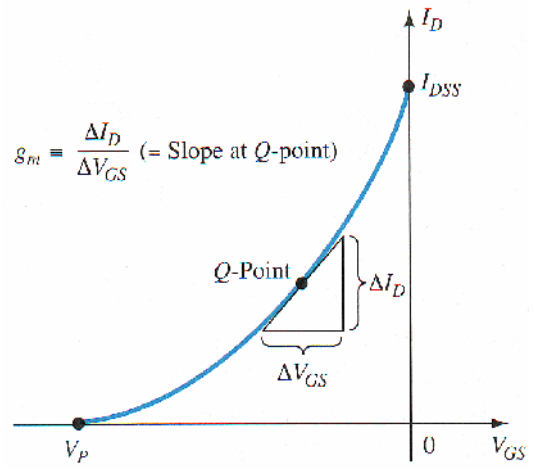


Fig-Definition of g_m using transfer characteristics

Example1: *Determine* g_m *for the JFET with* I_{DSS} *= 8mA &* V_P *= -4 at the following dc bias point: (a)* V_{GS} *= -0.5V,(b)* V_{GS} *= -1.5V,(c)* V_{GS} *= -2.5V*

Solution:

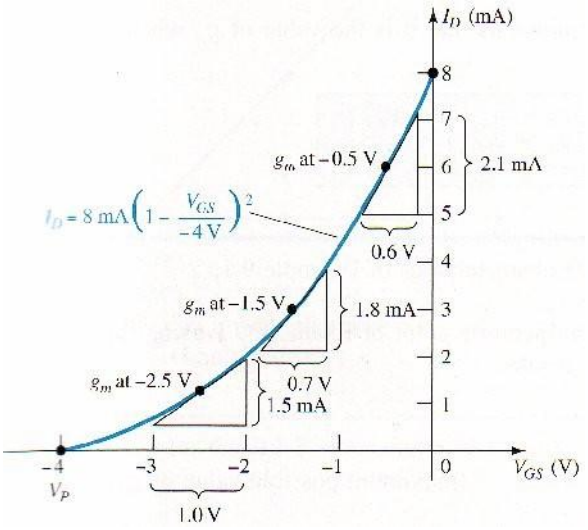


Fig-calculating g_m *at various bias points*

$$(a)gm = \frac{\Delta I_D}{\Delta V_{GS}} \simeq \frac{2.1\text{ mA}}{0.6\text{ V}} = \mathbf{3.5\text{ mS}}$$

$$(b)gm = \frac{\Delta I_D}{\Delta V_{GS}} \cong \frac{1.8\text{ mA}}{0.7\text{ V}} \cong \mathbf{2.57\text{ mS}}$$

$$(c)gm = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{1.5\text{ mA}}{1.0\text{ V}} = \mathbf{1.5\text{ mS}}$$

Mathematical Definition of g_m

The derivative of a function at a point is equal to the slope of the tangent line drawn at that point.

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{Q\text{-pt.}} = \left.\frac{dI_D}{dV_{GS}}\right|_{Q\text{-pt.}} = \frac{d}{dV_{GS}}\left[I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2\right]$$

$$= I_{DSS}\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$= 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[\frac{d}{dV_{GS}}(1) - \frac{1}{V_P}\frac{dV_{GS}}{dV_{GS}}\right] = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[0 - \frac{1}{V_P}\right]$$

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]$$

The maximum value of g_m for a JFET in which I_{DSS} and V_P have been specified

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{0}{V_P}\right]$$

$$g_{m0} = \frac{2I_{DSS}}{|V_P|}$$

means the value of $\boldsymbol{g_m}$ when V_{GS} = 0 V, then becomes

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right]$$

Example2: *For the JFET having the transfer char-of Ex1:*

(a) find the maximum value of g_m

(b) find the value of g_m *at each operating point . compare with graphical result*

Solution:

a) $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(8\text{ mA})}{4\text{ V}} = \mathbf{4\text{ mS}}$ (maximum possible value of g_m)

b) At $V_{GS} = -0.5$ V,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-0.5\text{ V}}{-4\text{ V}}\right] = \mathbf{3.5\text{ mS}}$$

At $V_{GS} = -1.5$ V,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-1.5\text{ V}}{-4\text{ V}}\right] = \mathbf{2.5\text{ mS}}$$

At $V_{GS} = -2.5$ V,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-2.5\text{ V}}{-4\text{ V}}\right] = \mathbf{1.5\text{ mS}}$$

On specification sheet, ***g_m*** *is provided as* ***y_{fs}*** *where* ***y*** *indicates it is part of an admittance equivalent circuit. The* ***f*** *signifies forward transfer parameter, and the* ***s*** *reveals that it is connected to the source terminal. In equation:*

$$g_m = y_{fs}$$

Plotting g_m vs. V_{GS}: *When V_{GS} is $1/2V_P$, g_m will be 1/2 the maximum value (g_{m0})*

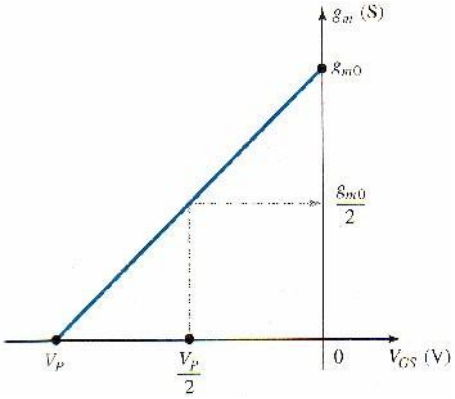


Fig - plot of g_m vs. V_{GS}

Example 3: *Plot g_m vs. V_{GS} for the JFET of Ex 1: and Ex 2:*

Solution:

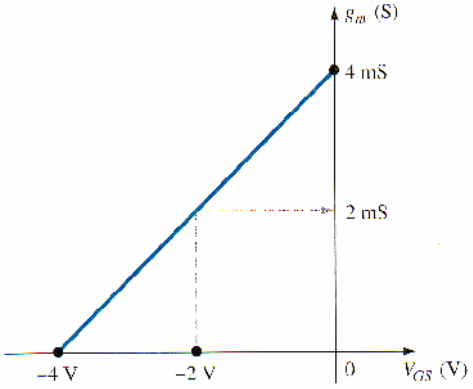


Fig-g_m vs. V_{GS}, with I_{DSS} = 8 mA & V_P = -4 V

Impact of I_D on g_m :

$$1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}}$$

Subs tituti ng

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right) = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}$$

Eq[9-8] into Eq.[9-6] will result in: *[*

(a) If $I_D = I_{DSS}$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}}{I_{DSS}}} = \mathbf{g_{m0}}$$

(b) If $I_D = I_{DSS}/2$,

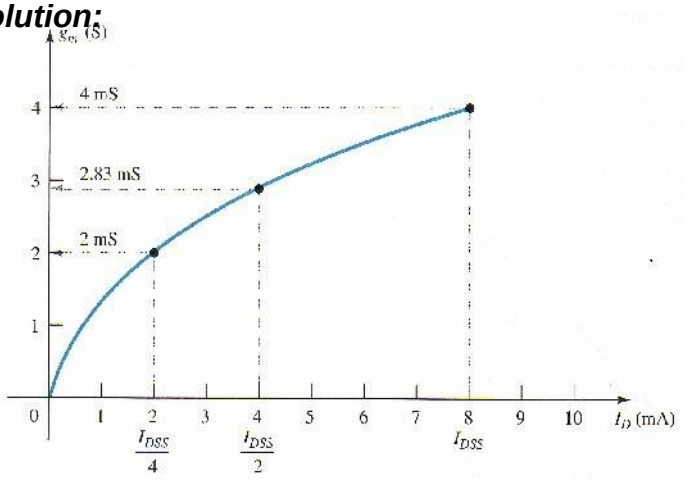
$$g_m = g_{m0}\sqrt{\frac{I_{DSS}/2}{I_{DSS}}} = \mathbf{0.707g_{m0}}$$

(c) If $I_D = I_{DSS}/4$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}/4}{I_{DSS}}} = \frac{g_{m0}}{2} = \mathbf{0.5g_{m0}}$$

Example 4: *Plot I_D vs. g_m for the JFET of Ex 1: through Ex 3:*

Solution:



$$Z_i\,(\text{FET}) = \propto \Omega$$

$$Z_o\,(\text{FET}) = r_d = \frac{1}{y_{os}}$$

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}\,=\,\text{constant}}$$

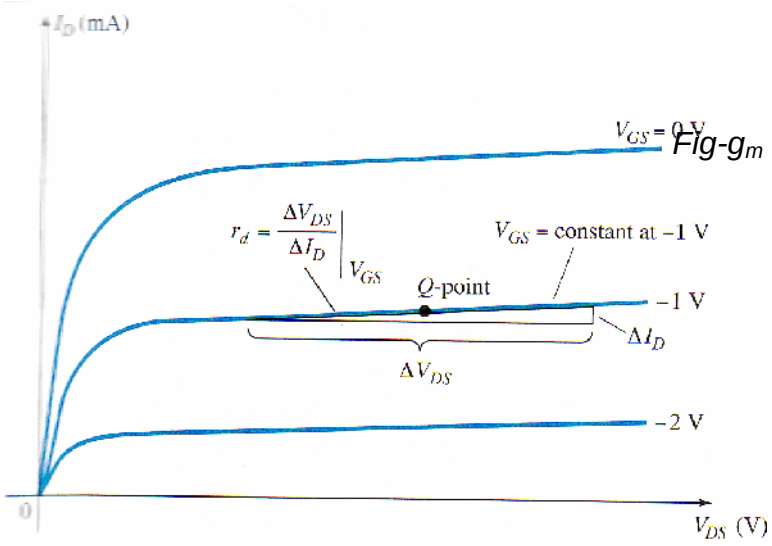


Fig-g_m vs. V_{GS}, I_{DSS} = 8mA & V_P = -4V

Fig- rd using FET drain char-

Example 5: *Determine the output impedance for the FET for V_{GS} = 0V,-2V, 8V*

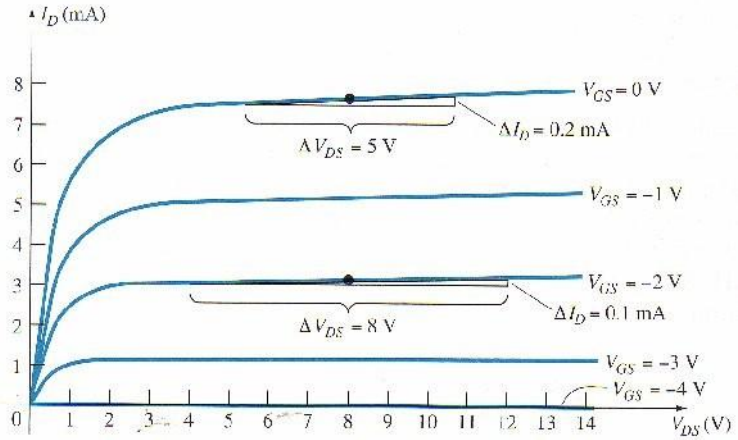


*Fig -Drain char-for r_d in **Ex5**:*

Solution: *For V_{GS}=0V, a tangent line is drawn and ΔV_{DS} is chosen as 5V, resulting in a ΔI_D of 0.2mA, substituting into Eq[9-12]*

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=0\text{ V}} = \frac{5\text{ V}}{0.2\text{ mA}} = 25\text{ k}\Omega$$

For V_{GS}=-2V, a tangent line is drawn and ΔV_{DS} is chosen as 8V, resulting in a ΔI_D of 0.1mA, substituting into Eq[9-12]

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=-2\text{ V}} = \frac{8\text{ V}}{0.1\text{ mA}} = 80\text{ k}\Omega$$

FET ac Equivalent Circuit

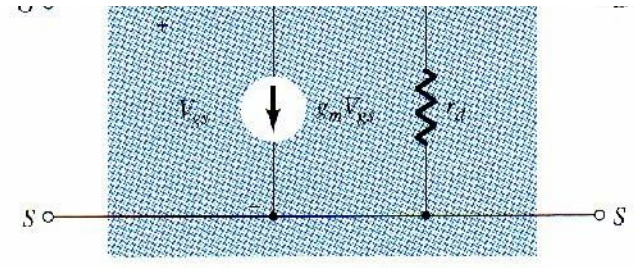


Fig-FET ac equivalent circuit

I_d *control by* ***V_{gs}*** *is a current source* ***$g_m V_{gs}$*** *connected from drain to source to establish a 180º phase shift*

Z_i *is open circuit at the input*

Z_o *is* ***r_d*** *from drain to source*

Example 6: *y_{fs} =3.8mS and y_{os} =20μS, Sketch the FET as equivalent model*

Solution:

$$g_m = y_{fs} = 3.8\ \text{mS} \quad \text{and} \quad r_d = \frac{1}{y_{os}} = \frac{1}{20\ \mu\text{S}} = 50\ \text{k}\Omega$$

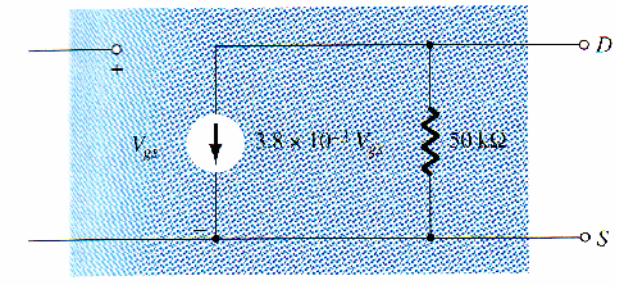


Fig-FET ac model for Ex6:

JFET Fixed-Bias Configuration (Common-Source)

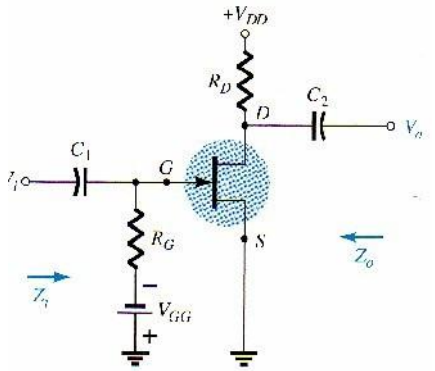


Fig-JFET fixed configuration

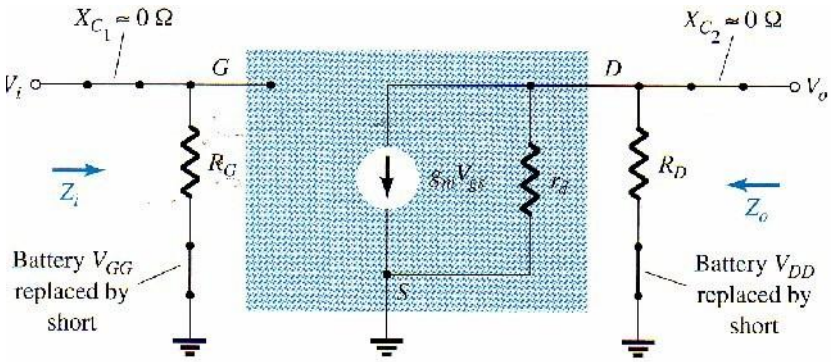
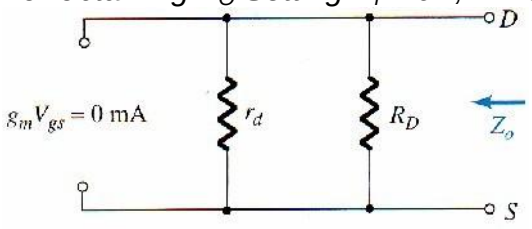


Fig-JFET ac equivalent

g_m & r_d determined from the dc biasing arrangement specification sheet, V_{GG} & V_{DD} are set to zero by a short circuit equivalent

Fig- Redrawn network

For obtaining Z_O Setting V_i = 0V, will establish V_{gs} as 0V also, this result $g_m V_{gs}$ = 0mA



$$Z_o = R_D \| r_d$$

$$Z_o \cong R_D \qquad r_d \geq 10R_D$$

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

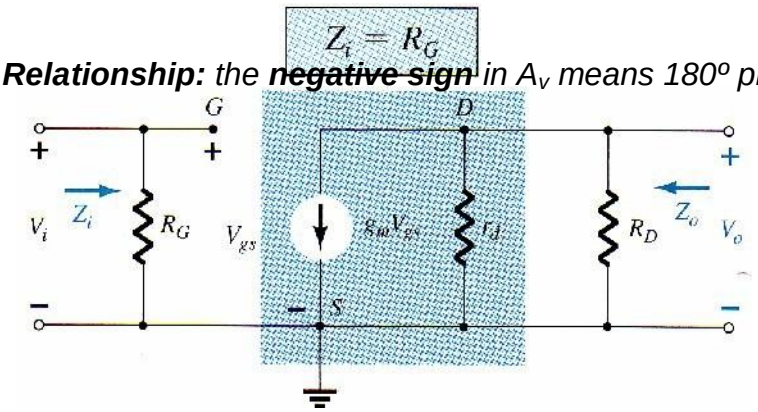
$$V_{gs} = V_i$$

$$V_o = -g_m V_i(r_d \| R_D)$$

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)$$

$$A_v = \frac{V_o}{V_i} = -g_m R_D \qquad r_d \geq 10R_D$$

Phase Relationship: *the* ***negative sign*** *in A_v means 180º phase shift between IP & OP*



Example 7: *configuration of Ex1: had V_{GSQ} = -2V & I_{DQ} = 5.625 mA, with I_{DSS} = 10 mA & V_p = -8V. The network is redrawn with an applied signal V_i, the value of y_{os} is provided as 40µs, Determine (a) g_m (b) r_d (c) Z_i (d) Z_o (e) A_v (f) A_v ignoring the effect of r_d*

Solution:

(a) $$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10\text{ mA})}{8\text{ V}} = 2.5\text{ mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.5\text{ mS}\left(1 - \frac{(-2\text{ V})}{(-8\text{ V})}\right) = \mathbf{1.88\text{ mS}}$$

(b) $$r_d = \frac{1}{y_{os}} = \frac{1}{40\ \mu\text{S}} = \mathbf{25\ k\Omega}$$

(c) $Z_i = R_G = \mathbf{1\ M\Omega}$

(d) $Z_o = R_D \| r_d = 2\text{ k}\Omega \| 25\text{ k}\Omega = \mathbf{1.85\ k\Omega}$

(e) $A_v = -g_m(R_D \| r_d) = -(1.88\text{ mS})(1.85\text{ k}\Omega)$
$= \mathbf{-3.48}$

(f) $A_v = -g_m R_D = -(1.88\text{ mS})(2\text{ k}\Omega) = \mathbf{-3.76}$

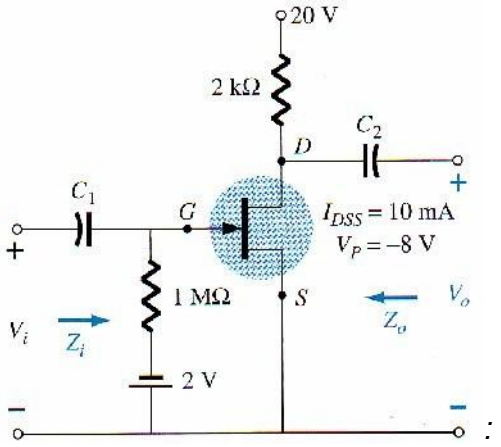


Fig-Ex7

JFET Self-Bias Configuration (Common-Source)
Bypassed R_S

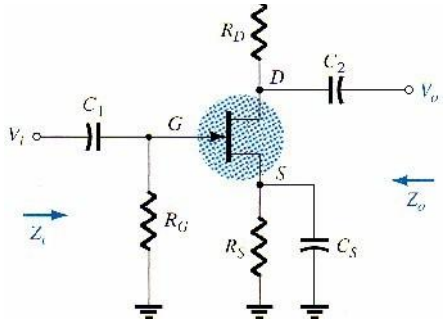


Fig- Self-bias JFET configuration

Since the resulting configuration i.e. Z_i, Z_o & A_v will be the same

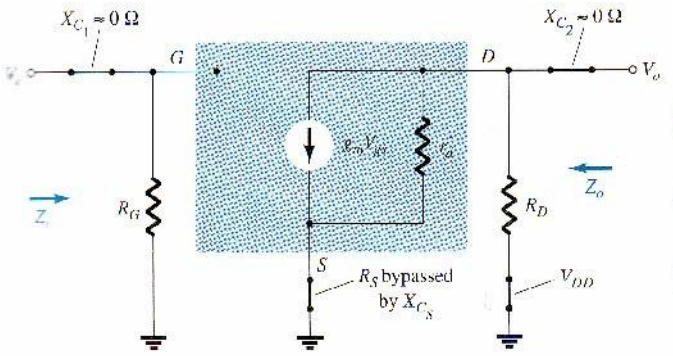


Fig - ac equivalent circuit

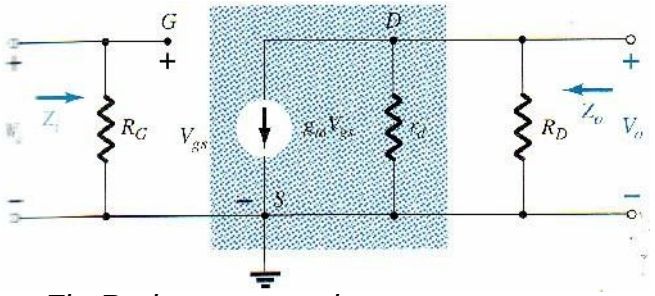


Fig-Redrawn network

$$Z_i = R_G$$

$$Z_o = r_d \| R_D$$

$$Z_o \cong R_D \qquad r_d \geq 10R_D$$

$$A_v = -g_m(r_d \| R_D)$$

$$A_v = -g_m R_D \qquad r_d \geq 10R_D$$

Phase Relationship: *the* ***negative sign*** *in A_v means 180º phase shift between IP & OP*

Un-bypassed R_S

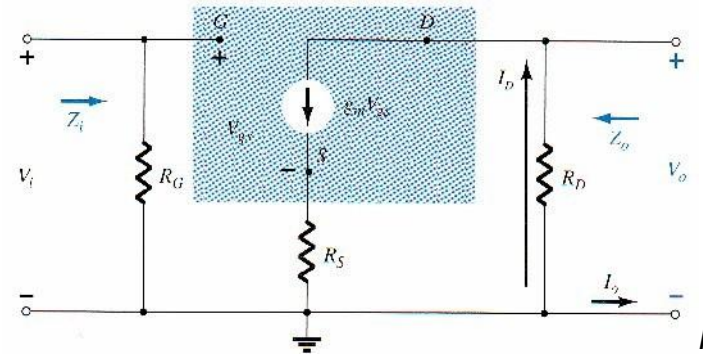


Fig-JFET with effect of R_S with r_d=∞Ω

Due to the open-circuit condition between the gate and the output network

$$Z_i = R_G$$

$$Z_o = \left.\frac{V_o}{I_o}\right|_{V_i=0}$$

Setting V_i=0V will result in the gate terminal being at ground potential(0V).The voltage across R_G is 0V, R_G "shorted out" of the picture. Applying KCL will result

$$I_o + I_D = g_m V_{gs}$$

$$V_{gs} = -(I_o + I_D)R_S$$

$$I_o + I_D = -g_m(I_o + I_D)R_S = -g_m I_o R_S - g_m I_D R_S$$

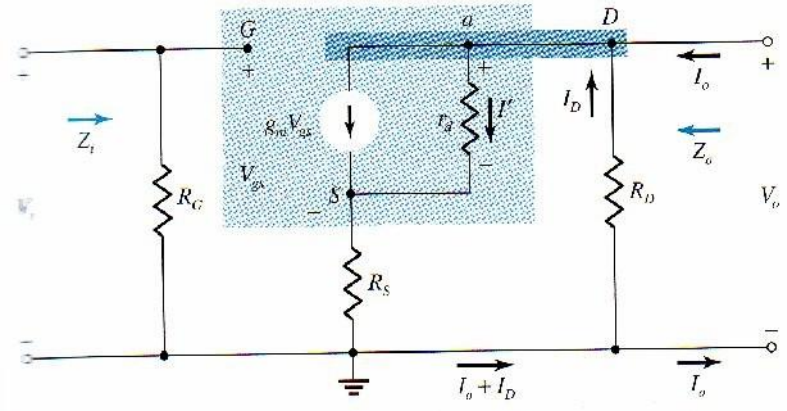
$$I_o[1 + g_m R_S] = -I_D[1 + g_m R_S]$$

$$V_o = -I_D R_D$$

$$V_o = -(-I_o)R_D = I_o R_D$$

$$Z_o = \frac{V_o}{I_o} = R_D \qquad r_d = \infty\ \Omega$$

If r_d is included in the network, the equivalent will appear as shown in fig9-18



$$Z_o = \left.\frac{V_o}{I_o}\right|_{V_i=0\text{ V}} = -\frac{I_D R_D}{I_o}$$

Fig9-18 r_d effect in self-bias JFET

We try to find an expression for I_o in terms of I_D applying KCL:

A_v: *for the network of fig9-18, applications of KVL on the input circuit result in:*

$$V_i - V_{gs} - V_{R_s} = 0$$

$$V_{gs} = V_i - I_D R_S$$

Voltage across r_d applying KVL

$$I_o = \frac{-I_D\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]}{1 + g_m R_S + \frac{R_S}{r_d}} \qquad I' = \frac{V_o - V_{R_S}}{r_d}$$

Applying KCL will result

$$Z_o = \frac{V_o}{I_o} = \frac{-I_D R_D}{-I_D\left(1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right)}$$

$$1 + g_m R_S + \frac{R_S}{r_d}$$

$$I_D = g_m V_{gs} + \frac{V_o - V_{R_S}}{r_d}$$

Substituting for V_{gs} from above and substituting for V_o and V_{RS} we have

$$Z_o = \left[1 + g\right] R_D$$

$$\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]$$

For $r_d \geq 10R_D$, $\left(1 + g_m R_S + \frac{R_S}{r_d}\right) \gg \frac{R_D}{r_d}$ and $1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}$

$\cong 1 + g_m R_S + \frac{R_S}{r_d}$ and

$$Z_o = R_D \quad r_d \geq 10R_D$$

$$I_D = g_m[V_i - I_D R_S] + \frac{(-I_D R_D) - (I_D R_S)}{r_d}$$

$$I_D\left[1 + g_m R_S + \frac{R_D + R_S}{r_d}\right] = g_m V_i$$

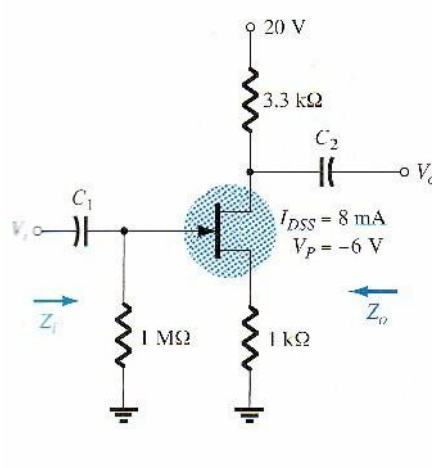
$$I_D = \frac{g_m V_i}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$$

The output voltage V_o is

$$= -I_D R_D = -\frac{g_m R_D V_i}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$$

Phase Relationship: *the* ***negative sign*** *in A_v means 180º phase shift between IP & OP*

Example 8: *configuration of fig9-19 has V_{GSQ}=-2.6V & I_{DQ}=2.6mA, with I_{DSS}=8mA & V_P=-6V. The network is redrawn as fig9-20 with an applied signal V_i. The value of y_{os} is given as 20μS, Determine (a) g_m (b) r_d (c) Z_i (d) Z_o with and without r_d (e) A_v with and without r_d*



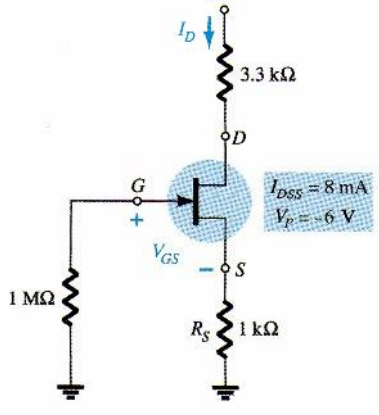


Fig-Ex8 *Fig-Redrawn Ex8:*

Solution:

(a) $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(8\text{ mA})}{6\text{ V}} = 2.67\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.67\text{ mS}\left(1 - \frac{(-2.6\text{ V})}{(-6\text{ V})}\right) = \mathbf{1.51\text{ mS}}$$

(b) $r_d = \dfrac{1}{y_{os}} = \dfrac{1}{20\ \mu\text{S}} = \mathbf{50\ k\Omega}$

(c) $Z_i = R_G = \mathbf{1\ M\Omega}$

(d) With r_d:

$$r_d = 50\text{ k}\Omega > 10R_D = 33\text{ k}\Omega$$

Therefore,

$$Z_o = R_D = \mathbf{3.3\ k\Omega}$$

If $r_d = \infty\ \Omega$

$$Z_o = R_D = \mathbf{3.3\ k\Omega}$$

(e) With r_d:

$$A_v = \frac{-g_m R_D}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}} = \frac{-(1.51\text{ mS})(3.3\text{ k}\Omega)}{1 - (1.51\text{ mS})(1\text{ k}\Omega) + \dfrac{3.3\text{ k}\Omega + 1\text{ k}\Omega}{50\text{ k}\Omega}}$$

$$= \mathbf{-1.92}$$

Without r_d:

$$A_v = \frac{-g_m R_D}{1 + g_m R_S} = \frac{-(1.51\text{ mS})(3.3\text{ k}\Omega)}{1 + (1.51\text{ mS})(1\text{ k}\Omega)} = \mathbf{-1.98}$$

3-JFET Voltage-Divide Configuration (Common-Source)

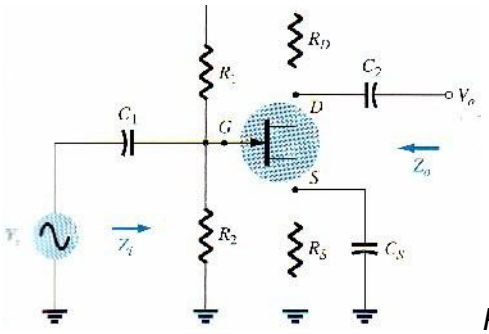


Fig- JFET voltage-divider configuration

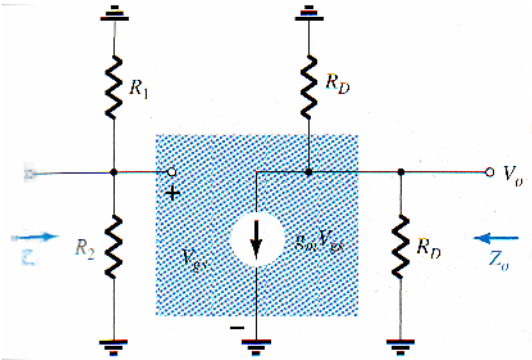


Fig- Network under ac conditions

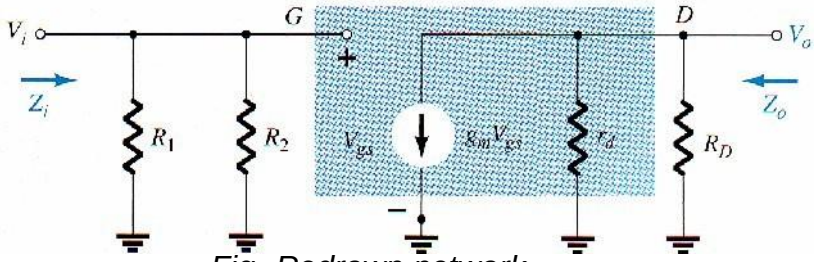


Fig- Redrawn network

$$Z_i = R_1 \| R_2$$

$$Z_o = r_d \| R_D$$

$$Z_o \cong R_D \qquad r_d \geq 10R_D$$

$$V_{gs} = V_i$$

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

$$A_v = \frac{V_o}{V_i} = \frac{-g_m V_{gs}(r_d \| R_D)}{V_{gs}}$$

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)$$

$$A_v = \frac{V_o}{V_i} \cong -g_m R_D \qquad r_d \geq 10R_D$$

4-JFET Source-Follower (Common-Drain Configuration)

The output is taken off the source terminal and when the dc supply is replaced by it's short-circuit equivalent, the drain is grounded (hence, the terminology common-drain)

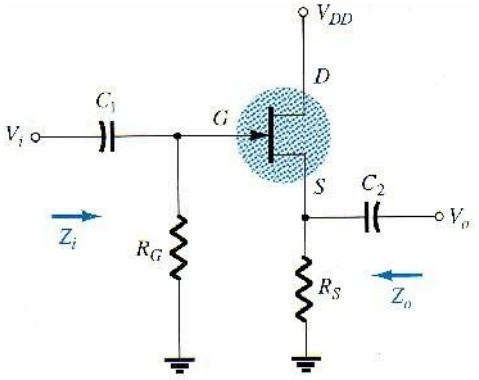


Fig-JFET Source-Follower configuration

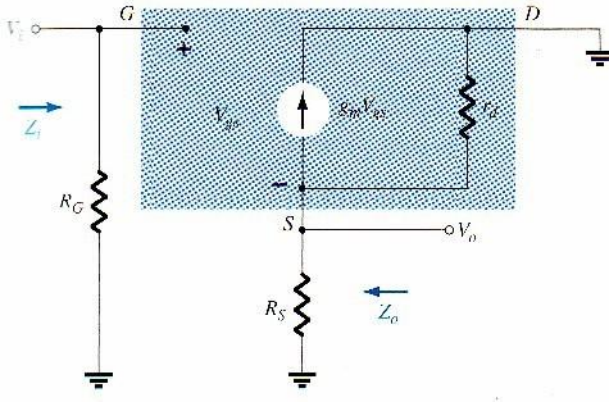


Fig-JFET ac equivalent model

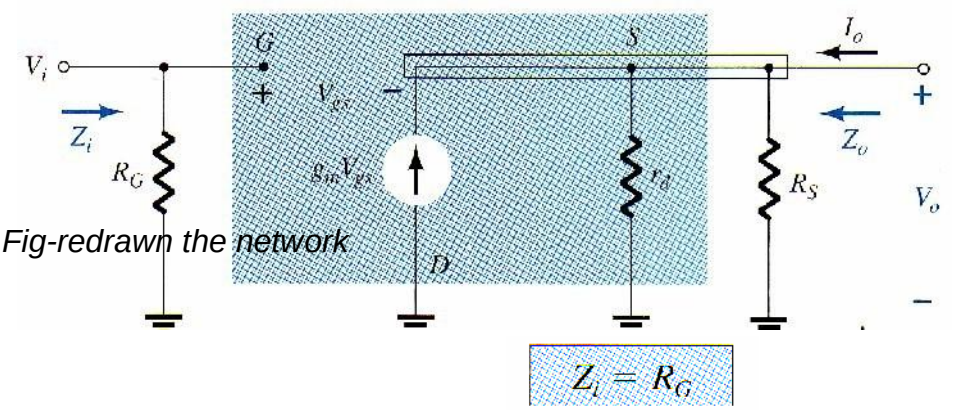
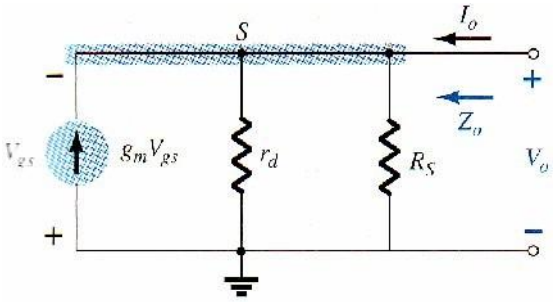


Fig-redrawn the network

Setting V_i = 0V will result in the gate terminal being connected directly to ground so that Z_o=

$V_o = -V_{gs}$ *applying KCL at node S*



$$I_o + g_m V_{gs} = I_{r_d} + I_{R_S}$$

$$= \frac{V_o}{r_d} + \frac{V_o}{R_S}$$

$$I_o = V_o\left[\frac{1}{r_d} + \frac{1}{R_S}\right] - g_m V_{gs}$$

$$= V_o\left[\frac{1}{r_d} + \frac{1}{R_S}\right] - g_m[-V_o]$$

$$= V_o\left[\frac{1}{r_d} + \frac{1}{R_S} + g_m\right]$$

$$Z_o = \frac{V_o}{I_o} = \frac{V_o}{V_o\left[\frac{1}{r_d} + \frac{1}{R_S} + g_m\right]} = \frac{1}{\frac{1}{r_d} + \frac{1}{R_S} + g_m} = \frac{1}{\frac{1}{r_d} + \frac{1}{R_S} +}$$

$$Z_o = r_d \| R_S \| 1/g_m$$

$$Z_o \cong R_S \| 1/g_m \qquad r_d \geq 10R_S$$

$$V_o = g_m V_{gs}(r_d \| R_S)$$

Applying KVL around the perimeter of the network of fig9-26 will result in:

$$V_i = V_{gs} + V_o$$
$$V_{gs} = V_i - V_o$$
$$V_o = g_m(V_i - V_o)(r_d \| R_S)$$
$$V_o = g_m V_i(r_d \| R_S) - g_m V_o(r_d \| R_S)$$
$$V_o[1 + g_m(r_d \| R_S)] = g_m V_i(r_d \| R_S)$$

$$A_v = \frac{V_o}{V_i} = \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)}$$

$$A_v = \frac{V_o}{V_i} \cong \frac{g_m R_S}{1 + g_m R_S} \qquad r_d \geq 10R_S$$

Since the bottom of above Eq is larger than the numerator by a factor of one, the gain can never be equal to or greater than one

Phase Relationship: *since* ***A_v is a positive quantity****, V_o and V_i are in phase*

Example 9: *A dc analysis of fig will result in V_{GSQ} = -2.86V & I_{DQ}=4.56mA, Determine (a) g_m (b) r_d (c) Z_i (d) Z_o with and without r_d (e) A_v with and without r_d*

Solution:

a) $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(16\text{ mA})}{4\text{ V}} = 8\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 8\text{ mS}\left(1 - \frac{(-2.86\text{ V})}{(-4\text{ V})}\right) = \mathbf{2.28\text{ mS}}$$

b) $r_d = \dfrac{1}{y_{os}} = \dfrac{1}{25\ \mu\text{S}} = \mathbf{40\ k\Omega}$

c) $Z_i = R_G = \mathbf{1\ M\Omega}$

d) With r_d:

$$Z_o = r_d \| R_S \| 1/g_m = 40\text{ k}\Omega \| 2.2\text{ k}\Omega \| 1/2.28\text{ mS}$$
$$= 40\text{ k}\Omega \| 2.2\text{ k}\Omega \| 438.6\ \Omega$$
$$= \mathbf{362.52\ \Omega}$$

Without r_d

$$Z_o = R_S \| 1/g_m = 2.2\text{ k}\Omega \| 438.6\ \Omega = \mathbf{365.69\ \Omega}$$

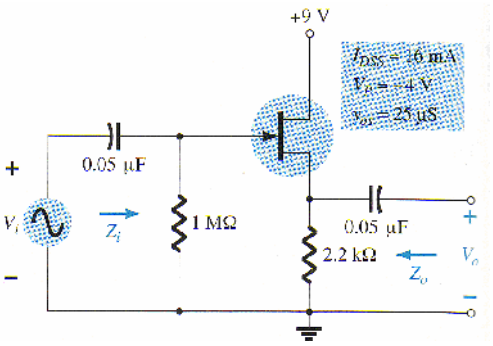


Fig- Ex9:

e) With r_d

$$A_v = \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)} = \frac{(2.28\text{ mS})(40\text{ k}\Omega \| 2.2\text{ k}\Omega)}{1 + (2.28\text{ mS})(40\text{ k}\Omega \| 2.2\text{ k}\Omega)}$$
$$= \frac{(2.28\text{ mS})(2.09\text{ k}\Omega)}{1 + (2.28\text{ mS})(2.09\text{ k}\Omega)} = \frac{4.77}{1 + 4.77} = \mathbf{0.83}$$

Without r_d:

$$A_v = \frac{g_m R_S}{1 + g_m R_S} = \frac{(2.28\ \text{mS})(2.2\ \text{k}\Omega)}{1 + (2.28\ \text{mS})(2.2\ \text{k}\Omega)}$$
$$= \frac{5.02}{1 + 5.02} = \mathbf{0.83}$$

Depletion-Type MOSFETs

The ac equivalent model for D-MOSFETs is exactly the same as that employed for JFETs as shown in fig9-28, the only difference is that V_{GSQ} can be positive for n-channel and negative for p-channel devices, the result is that g_m can be greater than g_{m0}

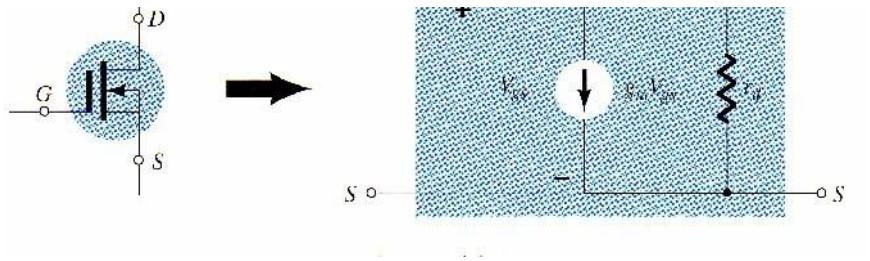


Fig- D-MOSFET ac circuit

Example 10: *The network of fig was analyzed, resulting in V_{GSQ} = 0.35V & I_{DQ} = 7.6mA, Determine (a) g_m and compare to g_{mo} (b) r_d (c) Sketch the ac equivalent network (d) Z_i (e) Z_o (f) A_v*

Solution:

(a) $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(6\text{ mA})}{3\text{ V}} = 4\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 4\text{ mS}\left(1 - \frac{(+0.35\text{ V})}{(-3\text{ V})}\right) = 4\text{ mS}(1 + 0.117) = \mathbf{4.47\text{ mS}}$$

(b) $r_d = \dfrac{1}{y_{os}} = \dfrac{1}{10\ \mu\text{S}} = \mathbf{100\ k\Omega}$

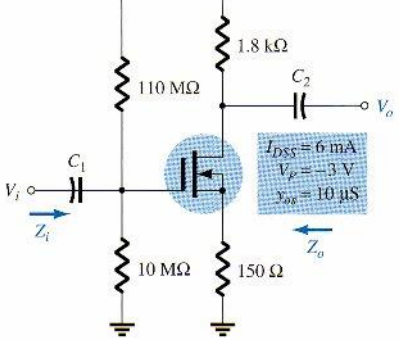


Fig-network for Ex10: (C)

See fig9-30 the similarities with the network of JFET fixed bias, self bias (bypassed) & voltage divider configuration so that the same Equation applied

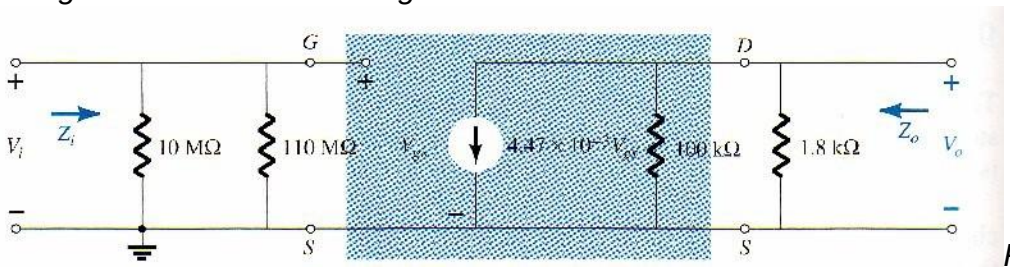


Fig-ac equivalent

Enhancement-Type MOSFETs

For the E-MOSFETs, the relationship between output current and controlling voltage is

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$

Fig 9-31 E-MOSFET ac circuit

$$g_m = \frac{dI_D}{dV_{GS}} = \frac{d}{dV_{GS}} k(V_{GS} - V_{GS(\text{Th})})^2 = k\frac{d}{dV_{GS}}(V_{GS} - V_{GS(\text{Th})})^2$$

$$= 2k(V_{GS} - V_{GS(\text{Th})})\frac{d}{dV_{GS}}(V_{GS} - V_{GS(\text{Th})}) = 2k(V_{GS} - V_{GS(\text{Th})})(1 - 0)$$

$$g_m = 2k(V_{GS} - V_{GS(\text{Th})})$$

Can be determined from a given typical operating point on a specification sheet

1- E-MOSFET Voltage Divider Configuration

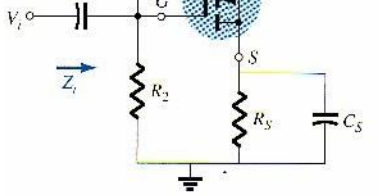
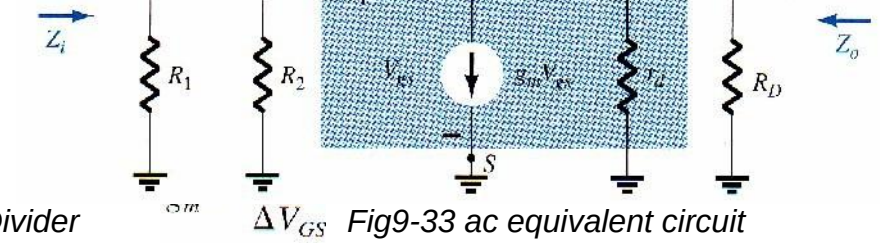
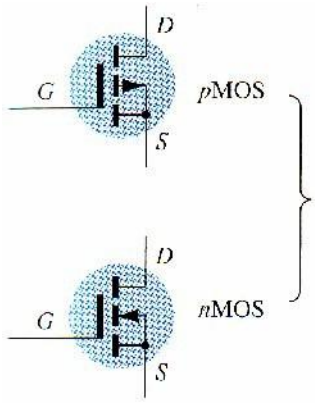
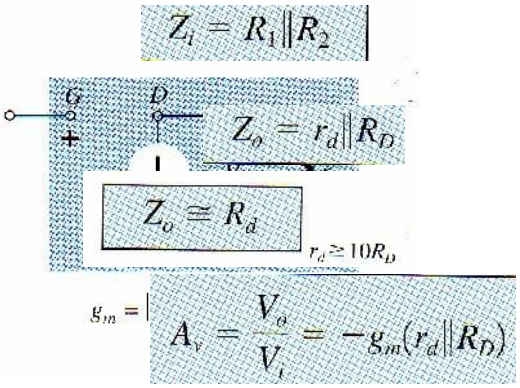


Fig9-32 E-MOSFET Voltage Divider



$g_m = \dfrac{\Delta I_D}{\Delta V_{GS}}$ *Fig9-33 ac equivalent circuit*





$$Z_i = R_1 \| R_2$$

$$Z_o = r_d \| R_D$$

$$Z_o \cong R_d$$

$r_d \geq 10R_D$

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)$$

$$A_v = \frac{V_o}{V_i} \cong -g_m R_D$$

Designing FET Amplifier Network

Example 12: *Design the fixed-bias network of fig9-34 to have an ac gain of 10, that is determining the value of R_D*

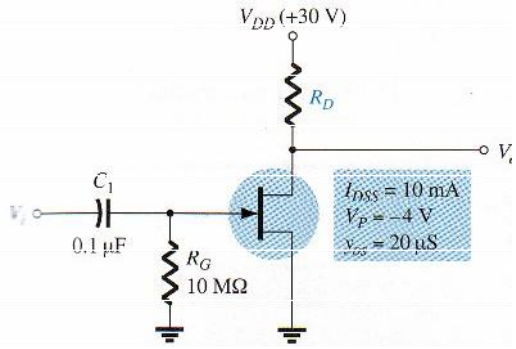


Fig- circuit for desired voltage gain in Ex11:

Solution:

$$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10\text{ mA})}{4\text{ V}} = 5\text{ mS}$$

$$-10 = -5\text{ mS}(R_D \| r_d)$$

$$R_D \| r_d = \frac{10}{5\text{ mS}} = 2\text{ k}\Omega$$

$$r_d = \frac{1}{y_{os}} = \frac{1}{20 \times 10^{-6}\text{ S}} = 50\text{ k}\Omega$$

$$R_D \| r_d = R_D \| 50\text{ k}\Omega = 2\text{ k}\Omega$$

$$\frac{R_D(50\text{ k}\Omega)}{R_D + 50\text{ k}\Omega} = 2\text{ k}\Omega$$

$$50R_D = 2(R_D + 50\text{ k}\Omega) = 2R_D + 100\text{ k}\Omega$$

$$48R_D = 100\text{ k}\Omega$$

$$R_D = \frac{100\text{ k}\Omega}{48} \cong 2.08\text{ k}\Omega$$

The closest standard value is 2KΩ, which would be employed for this region, the resulting level of V_{DSQ} would then be determined as follows:

$$V_{DS_Q} = V_{DD} - I_{D_Q}R_D = 30\text{ V} - (10\text{ mA})(2\text{ k}\Omega) = \mathbf{10\text{ V}}$$

Z_i and Z_o are set by the levels of R_G and R_D, respectively. That is,

$$Z_i = R_G = \mathbf{10\text{ M}\Omega}$$

$$Z_o = R_D \| r_d = 2\text{ k}\Omega \| 50\text{ k}\Omega = \mathbf{1.92\text{ k}\Omega} \cong R_D = 2\text{ k}\Omega$$

Example 13: *Choose the value of R_D and R_S for the network of fig 9-35 that will result in a gain of 8 using a relatively high level of g_m for this device defined at V_{GSQ} = 1/4 V_P*

Solution:

$$V_{GS_Q} = \frac{1}{4}V_P = \frac{1}{4}(-4\text{ V}) = -1\text{ V}$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS_Q}}{V_P}\right)^2 = 10\text{ mA}\left(1 - \frac{(-1\text{ V})}{(-4\text{ V})}\right)^2 = 5.625\text{ mA}$$

ing g_m,

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right)$$

$$= 5\text{ mS}\left(1 - \frac{(-1\text{ V})}{(-4\text{ V})}\right) = 3.75\text{ mS}$$

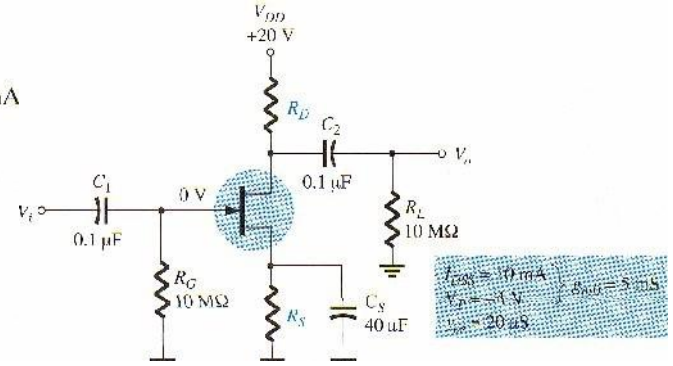


Fig-network for desired voltage gain

$$|A_v| = g_m(R_D \| r_d)$$

$$8 = (3.75\text{ mS})(R_D \| r_d)$$

$$R_D \| r_d = \frac{8}{3.75\text{ mS}} = 2.13\text{ k}\Omega$$

$$r_d = \frac{1}{y_{os}} = \frac{1}{20\ \mu\text{S}} = 50\text{ k}\Omega$$

$$R_D \| 50\text{ k}\Omega = 2.13\text{ k}\Omega$$

$$R_D = \mathbf{2.2\text{ k}\Omega}$$

$$V_{GS_Q} = -I_D R_S$$

$$-1\text{ V} = -(5.625\text{ mA})R_S$$

$$R_S = \frac{1\text{ V}}{5.625\text{ mA}} = 177.8\ \Omega$$

The closest standard value is 180Ω, in this example; R_S does not appear in the ac design because of the shorting effect of C_S

Example 13: *Determine R_D and R_S for the network of fig9-35 to establish a gain of 8 of the by-pass capacitor C_S is removed*

Solution: *V_{GSQ} and I_D are still -1V and 5.625mA, and since the equation V_{GS}=-$I_D R_S$ has not changed, R_S continues to equal the standard value of 180Ω*

$$A_v = -\frac{g_m R_D}{1 + g_m R_S}$$

$$|8| = \left|\frac{-(3.75\ \text{mS})R_D}{1 + (3.75\ \text{mS})(180\ \Omega)}\right| = \frac{(3.75\ \text{mS})R_D}{1 + 0.675}$$

$$8(1 + 0.675) = (3.75\ \text{mS})R_D$$

$$R_D = \frac{13.4}{3.75\ \text{mS}} = 3.573\ \text{k}\Omega$$

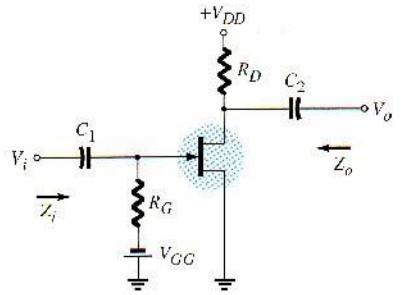
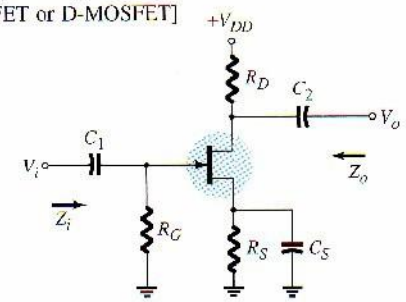
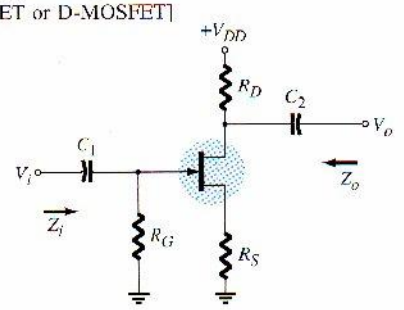
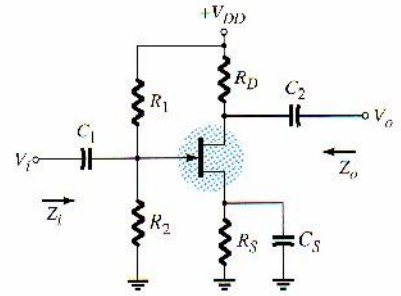
With the closest standard value at 3.6KΩ, we can now test the condition:

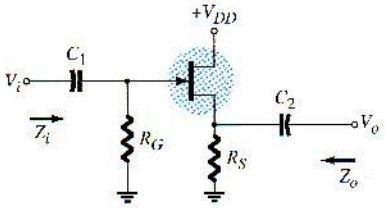
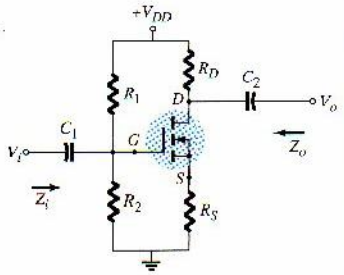
$$r_d \geq 10(R_D + R_S)$$

$$50\ \text{k}\Omega \geq 10(3.6\ \text{k}\Omega + 0.18\ \text{k}\Omega) = 10(3.78\ \text{k}\Omega)$$

$$50\ \text{k}\Omega \geq 37.8\ \text{k}\Omega$$

SUMMARY TABLE

Configuration	Z_i	Z_o	$A_v = \frac{V_o}{V_i}$
Fixed-bias [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(r_d \geq 10R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10R_D)$
Self-bias bypassed R_S [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(r_d \geq 10R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10R_D)$
Self-bias unbypassed R_S [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	$= \dfrac{\left[1 + g_m R_S + \frac{R_S}{r_d}\right] R_D}{\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]}$ $= R_D$ $r_d \geq 10R_D$ or $r_d = \infty\Omega$	Low (−2) $= \dfrac{g_m R_D}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$ $\cong -g_m R_D$ $[r_d \geq 10(R_D + R_S)]$
Voltage-divider bias [JFET or D-MOSFET] 	High (10 MΩ) $= R_1 \| R_2$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(r_d \geq 10R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10R_D)$

Configuration	Z_i	Z_o	$A_v = \frac{V_o}{V_i}$
Source-follower [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	Low (100 kΩ) $= r_d \| R_S \| 1/g_m$ $\cong R_S \| 1/g_m$ $(r_d \geq 10R_S)$	Low (< 1) $= \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)}$ $\cong \frac{g_m R_S}{1 + g_m R_S}$ $(r_d \geq 10R_S)$
Voltage-divider bias E-MOSFET 	Medium (1 MΩ) $= R_1 \| R_2$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(R_D \geq 10R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10R_D)$

Important Conclusion and Concept

1- The trans-conductance parameter g_m is determined by the ratio of the change in drain current associated with a particular change in gate-to-source voltage

2- On specification sheets, g_m is provided as y_{fs}

3-When V_{GS} is one-half the pinch-off value; g_m is one-half the maximum value

4- When I_D is one-fourth the saturation level of I_{DSS} , g_m is one-half the value at saturation

5- The output impedance of FETs is similar in magnitude to that of conventional BJTs

6- On specification sheets the output impedance r_d is provided as 1/ yos .

7- The voltage gain for the fixed-bias and self-bias JFET configurations (with a by passed source capacitance) is the same.

8- The ac analysis of JFETs and depletion-type MOSFETs is the same.

9- The ac equivalent network for E-MOSFETs is the same as that employed for the JFETs and D-MOSFETs, the only difference is the equation for g_m

10- The magnitude of the gain of FET networks is typically between 2 and 20. The self-bias configuration (without a bypass source capacitance) and the source follower are low-gain configurations

11- There is no phase shift between input and output for the source-follower

12- The output impedance for most FET configurations is determined primarily by R_D For the source-follower configuration it is determined by R_S and g_m

Equations

$$g_m = y_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}$$

$$g_{m0} = \frac{2I_{DSS}}{|V_P|}$$

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right]$$

$$g_m = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}$$

$$r_d = \frac{1}{y_{os}} = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=\text{constant}}$$

JFETs and depletion-type MOSFETs ($r_d \geq 10R_D$, $r_d \geq 10R_S$):

Fixed-bias:

$$Z_i = R_G$$
$$Z_o \cong R_D$$
$$A_v = -g_m R_D$$

Self-bias (bypassed R_S):

$$Z_i = R_G$$
$$Z_o \cong R_D$$
$$A_v = -g_m R_D$$

Self-bias (unbypassed R_S):

$$Z_i = R_G$$
$$Z_o = R_D$$
$$A_v \cong \frac{-g_m R_D}{1 + g_m R_S}$$

Voltage-divider bias:

$$Z_i = R_1 \| R_2$$
$$Z_o = R_D$$
$$A_v = -g_m R_D$$

Source-follower:

$$Z_i = R_G$$
$$Z_o = R_S \| 1/g_m$$
$$A_v = \frac{g_m R_S}{1 + g_m R_S}$$

Enhancement-type MOSFETs ($g_m = 2k(V_{GS_Q} - V_{GS(\text{Th})})$

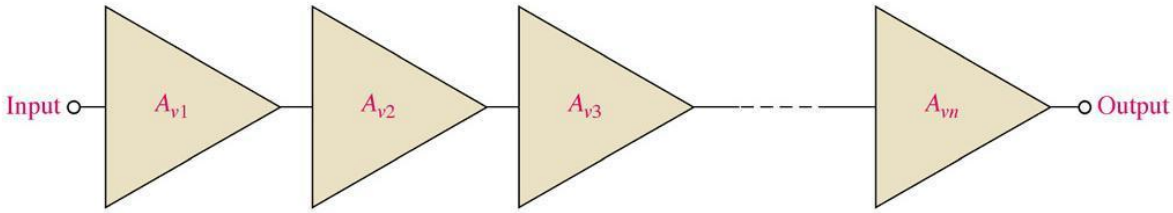
Voltage-divider bias:

$$Z_i = R_1 \| R_2$$
$$Z_o \cong R_D$$
$$A_v = -g_m R_D$$

Multistage Amplifiers

Two or more amplifiers can be connected to increase the gain of an ac signal. The overall gain can be calculated by simply multiplying each gain together.

$A'_v = A_{v1}A_{v2}A_{v3}$ ……



Multistage Amplifier Cutoff Frequencies and Bandwidth

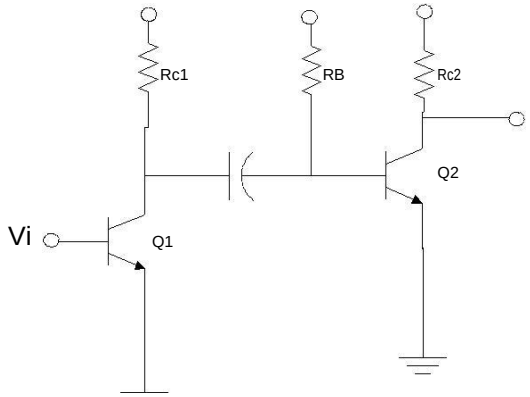
When amplifiers having equal cutoff frequencies are cascaded, the cutoff frequencies and bandwidth of the multistage circuit are found using .

$$f_{C\,2(T)} \quad f_{C\,2}\sqrt{2^{1/n}} \quad 1$$

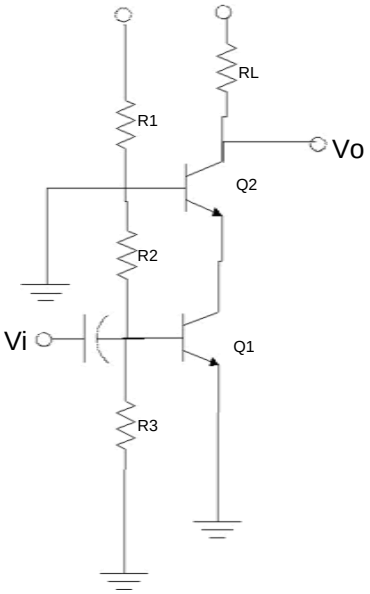
$$f_{C1(T)} \quad \frac{f_{C1}}{\sqrt{2^{1/n}1}}$$

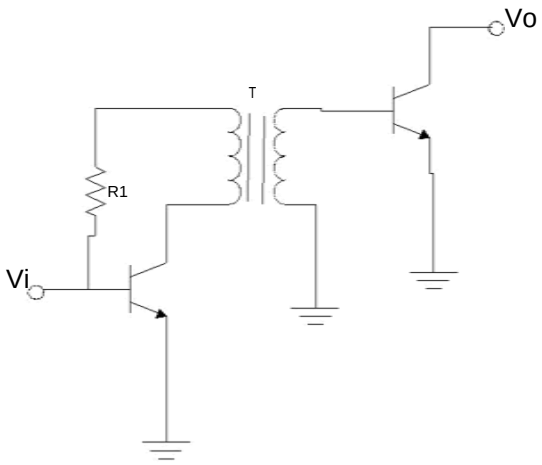
$$BW \quad f_{C\,2(T)} \quad f_{C1(T)}$$

Multistage amplifier configuration



Cascade /RC coupling





Cascode

Transformer coupling

Cascade Connection

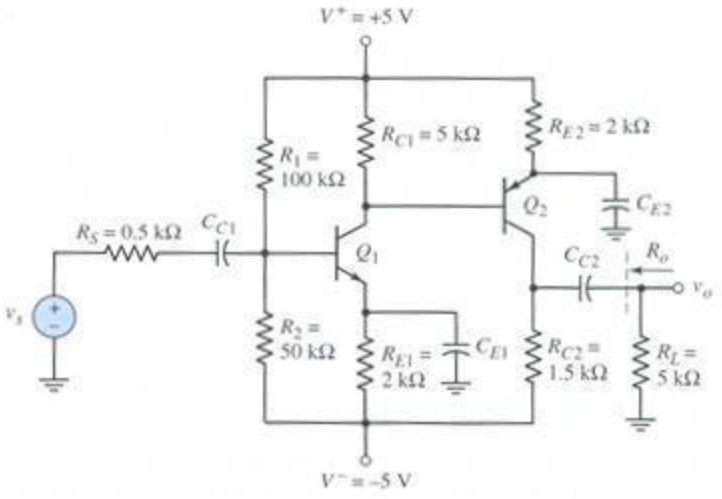
The most widely used method

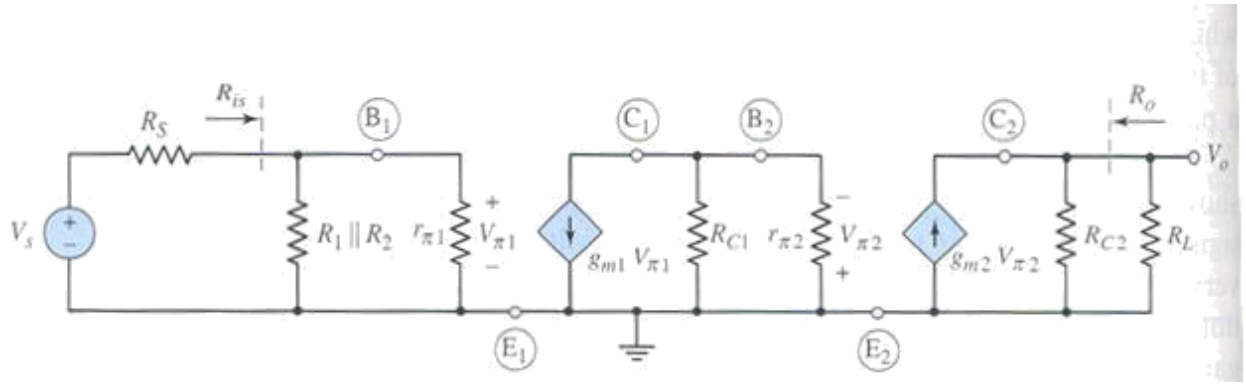
Coupling a signal from one stage to the another stage and block dc voltage from one stage to the another stage

The signal developed across the collector resistor of each stage is coupled into

the base of the next stage

The overall gain = product of the individual gain.





small signal gain is: by determine the voltage gain at stages 1 & stage 2

$$A_V = A_{V1} A_{V2}$$

$$A_V = \frac{V_0}{V_S} = g_{m1} g_{m2} (R_{C1} // r_2)(R_{C2} // R_L)\left(\frac{R_i}{R_i R_S}\right)$$

Gain in db

$$A_{V\,(dB)} = 20 \log(A_V)$$

input resistance

$$R_{is} = R_1 // R_2 // r_1$$

for output resistance

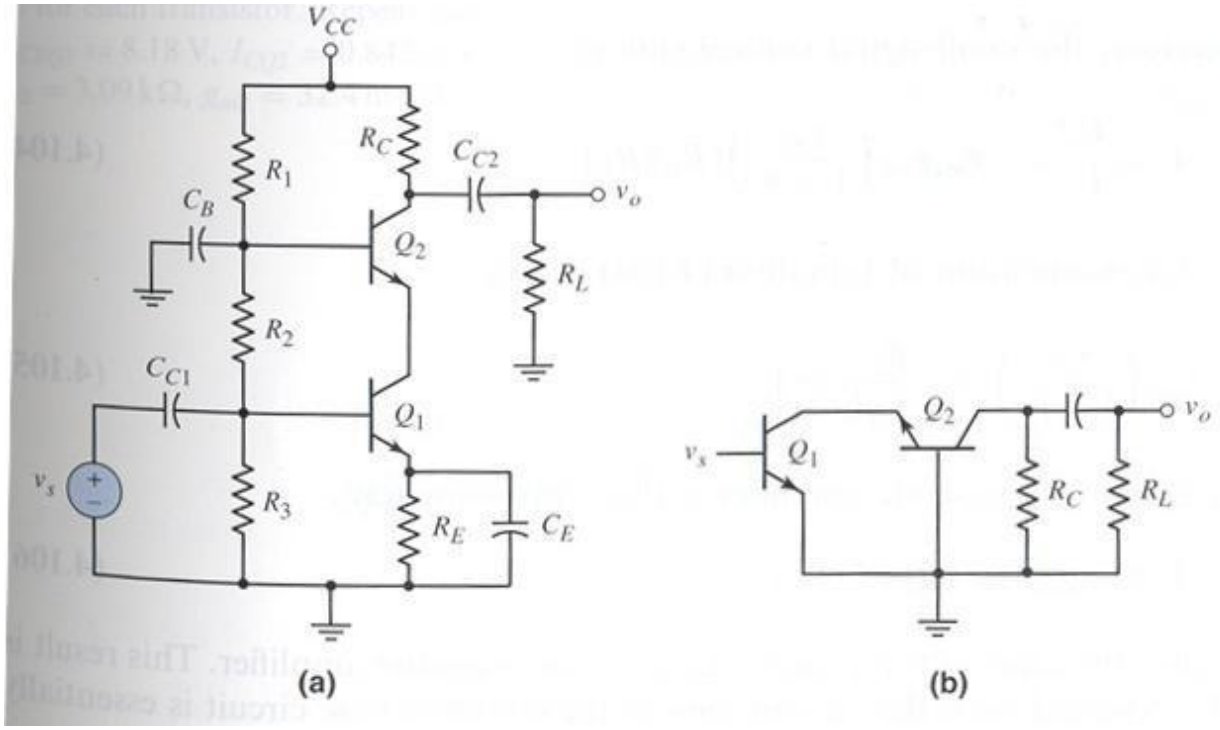
assume v_S=0 so $V_1 = V_2 = 0$ also $g_{m1} V_1 = g_{m2} V_2 = 0$ therefore $R_0 = R_{C2}$.

Cascode Connection:

A cascode connection has one transistor on top of (in series with) another -The i/p into a C-E amp. (Q1) is, which drives a C-B amp. (Q2)

-The o/p signal current of Q1 is the i/p signal of Q2

-The advantage: provide a high i/p impedance with low voltage gain to ensure the i/p Miller capacitance is at a min. with the C-B stage providing good high freq. operation.



From the small equivalent circuit, since the capacitors act as short circuit,

by KCL equation at E2:

$$g_{m1}V_1 \frac{V_2}{r_2} g_{m2}V_2$$

solving for voltage V_2

$$V_2 \quad \frac{r_2}{1_2} g_{m1}V_S$$

Where

$$2 \quad g_{m2} r_2$$

the output voltage is

$$V_o \quad (g_{m2}V_2)(R_C // R_L)$$

or

$$\frac{r_2}{1_2} \quad // R_L)V_S$$

Therefore the small signal voltage gain:

$$A_V \quad \frac{V_0}{V_S} g_{m1} g_{m2} \quad \frac{r_2}{1_2} R_C \quad // R_L$$

From above equation shows that:

$$g_{m2} \quad \frac{r_2}{1_2} \quad \frac{2}{1_2} 1$$

So, the cascode gain is the approximately

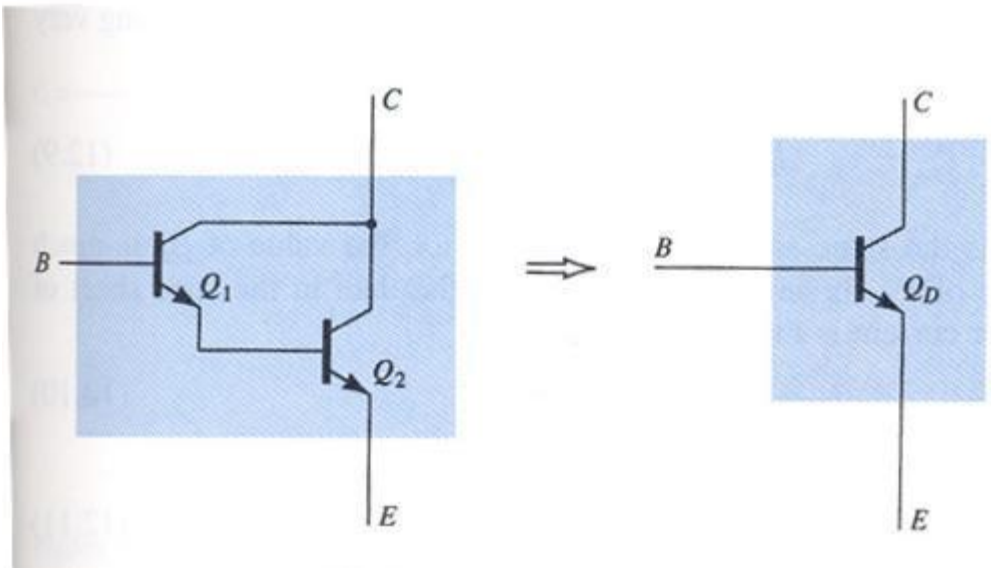
$$A_V \quad g_{m1} \; R_C \,//\, R_L$$

* The gain same as a single-stage C-E amplifier

Darlington Connection

The main feature is that the composite transistor acts as a single unit with a current gain that is the product of the current gains of the individual transistors - Provide high current gain than a single BJT

-The connection is made using two separate transistors having current gains of $_1$ and $_2$.



So, the current gain $_D$ $_1$ $_2$

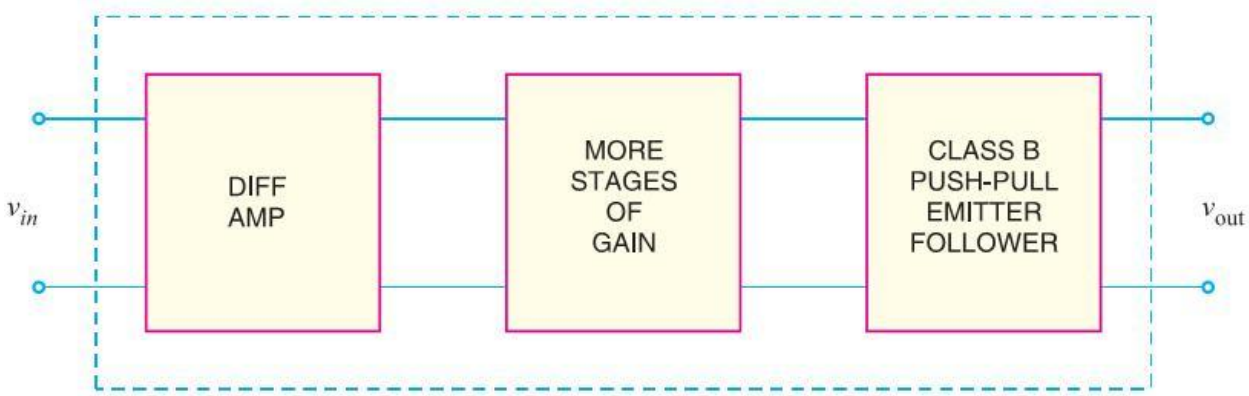
If $_1$ $_2$

The Darlington connection provides a current gain of $_D$ ^{2}.

MODULE-IV

Operational amplifier

An operational amplifier(OP-Amp) is a circuit that can perform such mathematical operations as addition, subtraction, integration and differentiation. Fig.1 shows the block diagram of an operational amplifier. Note that OP-Amp is a multistage amplifier. The three stages are : differential amplifier input stage followed by a high-gain CEamplifier and finally the output stage.

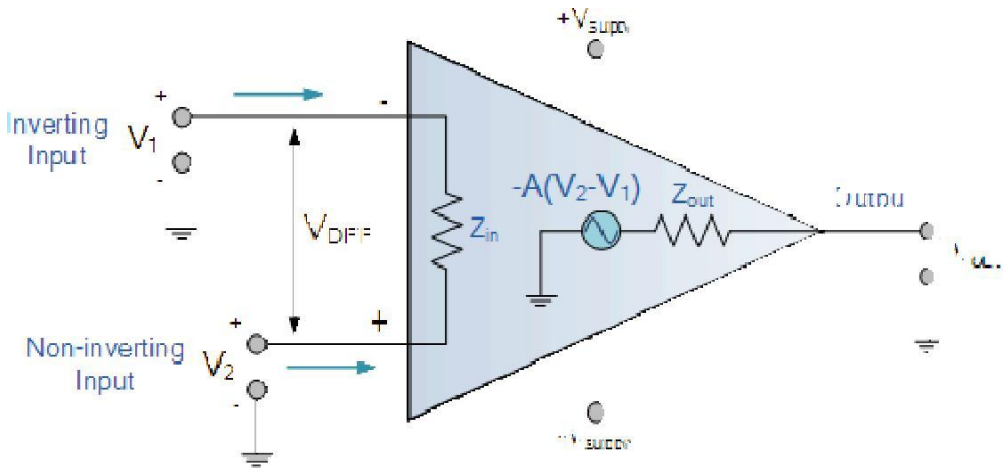


An **Operational Amplifier** is basically a three-terminal device which consists of two high impedance inputs, one called the **Inverting Input**, marked with a negative or “minus” sign, (-) and the other one called the **Non-inverting Input**, marked with a positive or “plus” sign (+).

The third terminal represents the Operational Amplifiers output port which can both sink and source either a voltage or a current. In a linear operational amplifier, the output signal is the amplification factor, known as the amplifiers gain (A) multiplied by the value of the input signal and depending on the nature of these input and output signals, there can be four different classifications of operational amplifier gain.

Voltage – Voltage “in” and Voltage “out”
Current – Current “in” and Current “out”
Transconductance – Voltage “in” and Current “out”
Transresistance – Current “in” and Voltage “out”

Equivalent Circuit of an Ideal Operational Amplifier



Op-amp Parameter and Idealised Characteristic

Open Loop Gain, (Avo)

Infinite – The main function of an operational amplifier is to amplify the input signal and the more open loop gain it has the better. Open-loop gain is the gain of the op-amp without positive or negative feedback and for such an amplifier the gain will be infinite but typical real values range from about 20,000 to 200,000.

Input impedance, (Z_{in})

- **Infinite** – Input impedance is the ratio of input voltage to input current and is assumed to be infinite to prevent any current flowing from the source supply into the amplifiers input circuitry (Iin = 0). Real op-amps have input leakage currents from a few pico-amps to a few milli-amps.

Output impedance, (Z_{out})

- **Zero** – The output impedance of the ideal operational amplifier is assumed to be zero acting as a perfect internal voltage source with no internal resistance so that it can supply as much current as necessary to the load. This internal resistance is effectively in series with the load thereby reducing the output voltage available to the load. Real op-amps have output impedances in the 100-20k range.

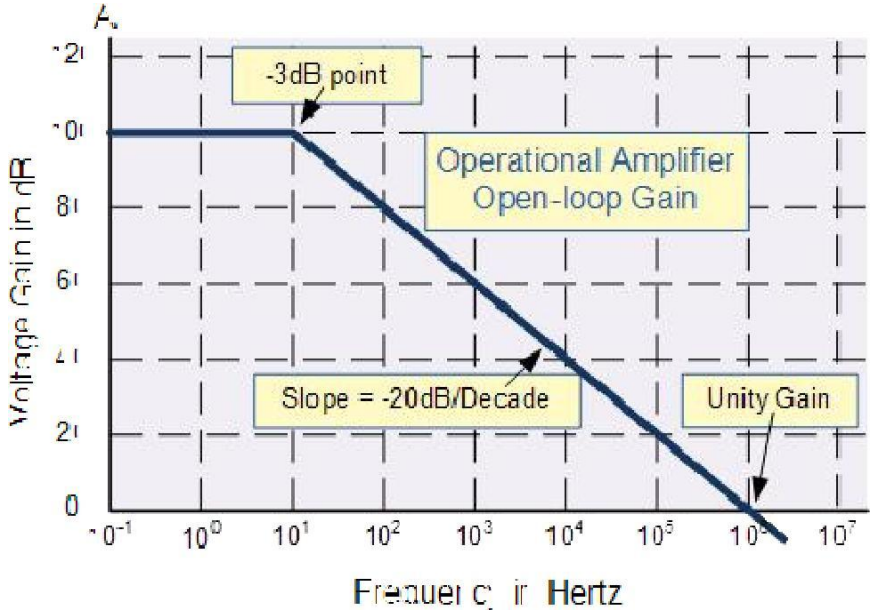
Bandwidth, (BW)

Infinite – An ideal operational amplifier has an infinite frequency response and can amplify any frequency signal from DC to the highest AC frequencies so it is therefore assumed to have an infinite bandwidth. With real op-amps, the bandwidth is limited by the Gain-Bandwidth product (GB), which is equal to the frequency where the amplifiers gain becomes unity.

Offset Voltage, (V_{io})

- **Zero** – The amplifiers output will be zero when the voltage difference between the inverting and the non-inverting inputs is zero, the same or when both inputs are grounded. Real op-amps have some amount of output offset voltage.

Open-loop Frequency Response Curve



From this frequency response curve we can see that the product of the gain against frequency is constant at any point along the curve. Also that the unity gain (0dB) frequency also determines the gain of the amplifier at any point along the curve. This constant is generally known as the **Gain Bandwidth Product** or **GBP**. Therefore:

GBP = Gain x Bandwidth or A x BW.

The **Voltage Gain** (A_V) of the operational amplifier can be found using the following formula:

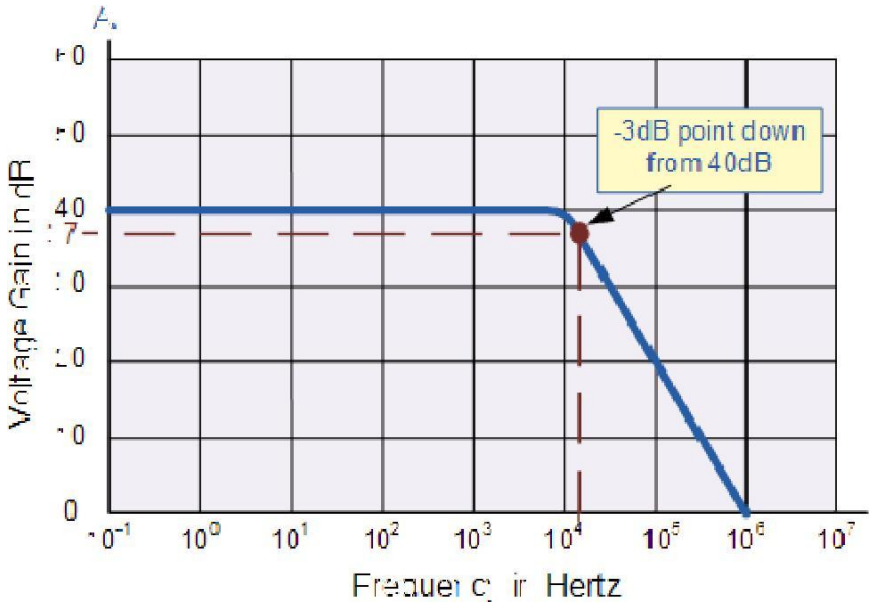
$$\text{Voltage Gain, } A = \frac{V_{out}}{V_{in}}$$

and in **Decibels** or (dB) is given as:

$$20 \log |A| \text{ or } 20 \log \frac{V_{out}}{V_{in}} \text{ in dB}$$

An Operational Amplifiers Bandwidth

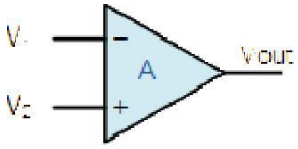
The operational amplifiers bandwidth is the frequency range over which the voltage gain of the amplifier is above **70.7%** or **-3dB** (where 0dB is the maximum) of its maximum output value as shown below.



Here we have used the 40dB line as an example. The -3dB or 70.7% of Vmax down point from the frequency response curve is given as **37dB**. Taking a line across until it intersects with the main GBP curve gives us a frequency point just above the 10kHz line at about 12 to 15kHz. We can now calculate this more accurately as we already know the GBP of the amplifier, in this particular case 1MHz.

Operational Amplifiers Summary

We know now that an **Operational amplifiers** is a very high gain DC differential amplifier that uses one or more external feedback networks to control its response and characteristics. We can connect external resistors or capacitors to the op-amp in a number of different ways to form basic “building Block” circuits such as, Inverting, Non-Inverting, Voltage Follower, Summing, Differential, Integrator and Differentiator type amplifiers.

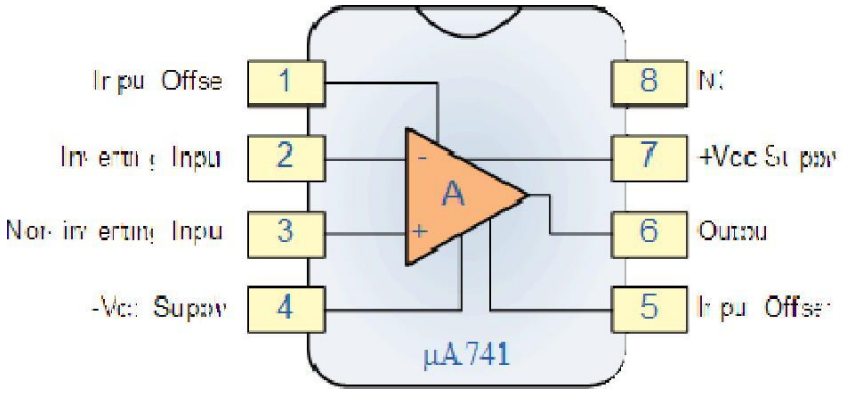


Op-amp Symbol

An “ideal” or perfect Operational Amplifier is a device with certain special characteristics such as infinite open-loop gain Ao, infinite input resistance Rin, zero output resistance Rout, infinite bandwidth 0 to and zero offset (the output is exactly zero when the input is zero).

There are a very large number of operational amplifier IC’s available to suit every possible application from standard bipolar, precision, high-speed, low-noise, high-voltage, etc, in either standard configuration or with internal Junction FET transistors.

Operational amplifiers are available in IC packages of either single, dual or quad op-amps within one single device. The most commonly available and used of all operational amplifiers in basic electronic kits and projects is the industry standard **A-741**.



In the next tutorial about Operational Amplifiers, we will use negative feedback connected around the op-amp to produce a standard closed-loop amplifier circuit called an Inverting Amplifier circuit that produces an output signal which is 180^{o} “out-of-phase” with the input.

The Inverting Operational Amplifier

As the open loop DC gain of an Operational Amplifiers is extremely high we can therefore afford to lose some of this high gain by connecting a suitable resistor across the amplifier from the output terminal back to the inverting input terminal to both reduce and control the overall gain of the amplifier. This then produces and effect known commonly as Negative Feedback, and thus produces a very stable Operational Amplifier based system.

Negative Feedback is the process of “feeding back” a fraction of the output signal back to the input, but to make the feedback negative, we must feed it back to the negative or “inverting input” terminal of the op-amp using an external **Feedback Resistor** called Rf. This feedback

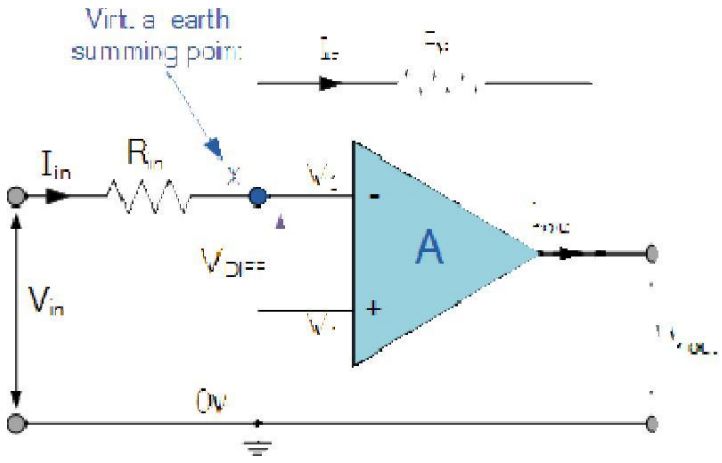
connection between the output and the inverting input terminal forces the differential input voltage towards zero.

This effect produces a closed loop circuit to the amplifier resulting in the gain of the amplifier now being called its **Closed-loop Gain**. Then a closed-loop inverting amplifier uses negative feedback to accurately control the overall gain of the amplifier, but at a cost in the reduction of the amplifiers gain.

This negative feedback results in the inverting input terminal having a different signal on it than the actual input voltage as it will be the sum of the input voltage plus the negative feedback voltage giving it the label or term of a *Summing Point*. We must therefore separate the real input signal from the inverting input by using an **Input Resistor**, Rin.

As we are not using the positive non-inverting input this is connected to a common ground or zero voltage terminal as shown below, but the effect of this closed loop feedback circuit results in the voltage potential at the inverting input being equal to that at the non-inverting input producing a *Virtual Earth* summing point because it will be at the same potential as the grounded reference input. In other words, the op-amp becomes a “differential amplifier”.

Inverting Operational Amplifier Configuration



In this **Inverting Amplifier** circuit the operational amplifier is connected with feedback to produce a closed loop operation. When dealing with operational amplifiers there are two very important rules to remember about inverting amplifiers, these are: “No current flows into the input terminal” and that “V1 always equals V2”. However, in real world op-amp circuits both of these rules are slightly broken.

This is because the junction of the input and feedback signal (X) is at the same potential as the positive (+) input which is at zero volts or ground then, the junction is a **“Virtual Earth”**. Because of this virtual earth node the input resistance of the amplifier is equal to the value of the

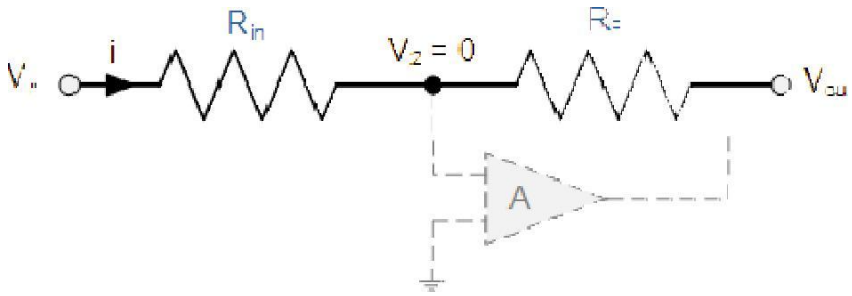
input resistor, Rin and the closed loop gain of the inverting amplifier can be set by the ratio of the two external resistors.

We said above that there are two very important rules to remember about **Inverting Amplifiers** or any operational amplifier for that matter and these are.

1. No Current Flows into the Input Terminals
2. The Differential Input Voltage is Zero as V1 = V2 = 0 (Virtual Earth)

Then by using these two rules we can derive the equation for calculating the closed-loop gain of an inverting amplifier, using first principles.

Current (i) flows through the resistor network as shown.



$$i = \frac{Vin - Vout}{Rin + Rf}$$

$$\text{Therefore, } i = \frac{Vin - V2}{Rin} = \frac{V2 - Vout}{Rf}$$

$$i = \frac{Vin}{Rin} - \frac{V2}{Rin} = \frac{V2}{Rf} - \frac{Vout}{Rf}$$

$$\text{i.e., } \frac{Vin}{Rin} = V2\left[\frac{1}{Rin} + \frac{1}{Rf}\right] - \frac{Vout}{Rf}$$

$$\text{and since, } i = \frac{Vin - 0}{Rin} = \frac{0 - Vout}{Rf} \qquad \frac{Rf}{Rin} = \frac{0 - Vout}{Vin - 0}$$

The Closed Loop Gain (Av) is given as, $\frac{Vout}{Vin} = -\frac{Rf}{Rin}$

Then, the **Closed-Loop Voltage Gain** of an Inverting Amplifier is given as.

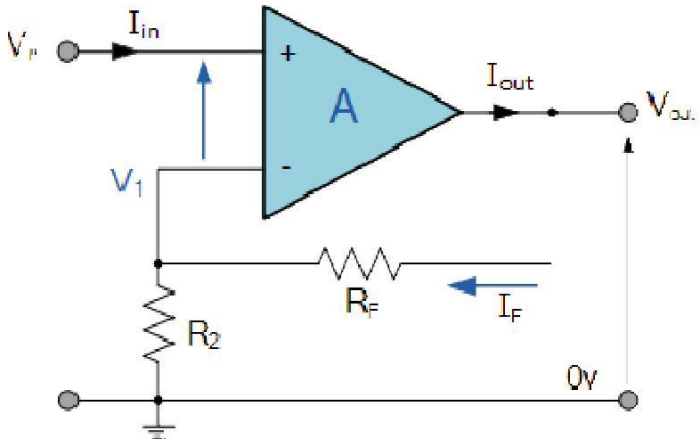
$$Gain\,(Av) = \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_{in}}$$

and this can be transposed to give Vout as:

$$V_{out} = -\frac{R_f}{R_{in}} \times V_{in}$$

The Non-inverting Operational Amplifier

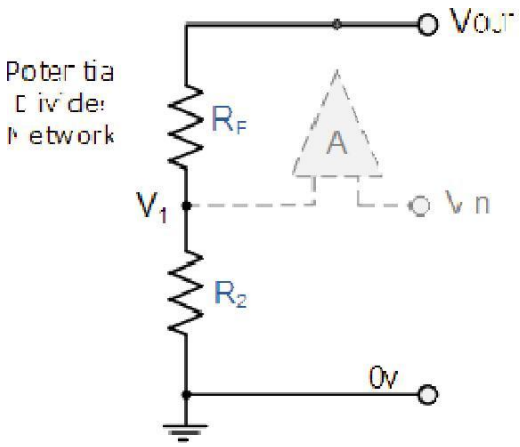
Non-inverting Operational Amplifier Configuration



In the previous Inverting Amplifier tutorial, we said that for an ideal op-amp "No current flows into the input terminal" of the amplifier and that "V1 always equals V2". This was because the junction of the input and feedback signal (V1) are at the same potential.

In other words the junction is a "virtual earth" summing point. Because of this virtual earth node the resistors, R*f* and R2 form a simple potential divider network across the non-inverting amplifier with the voltage gain of the circuit being determined by the ratios of R2 and R*f* as shown below.

Equivalent Potential Divider Network



Then using the formula to calculate the output voltage of a potential divider network, we can calculate the closed-loop voltage gain (A_V) of the **Non-inverting Amplifier** as follows:

$$V_{-} = \frac{R_2}{R_2 + R_F} \times V_{OUT}$$

$$\text{Ideal Summing Point: } V_{-} = V_{IN}$$

$$\text{Voltage Gain, } A_{(V)} \text{ is equal to: } \frac{V_{OUT}}{V_{IN}}$$

$$\text{Then, } A_{(V)} = \frac{V_{OUT}}{V_{IN}} = \frac{R_2 + R_F}{R_2}$$

$$\text{Transposed to give: } A_{(V)} = \frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_F}{R_2}$$

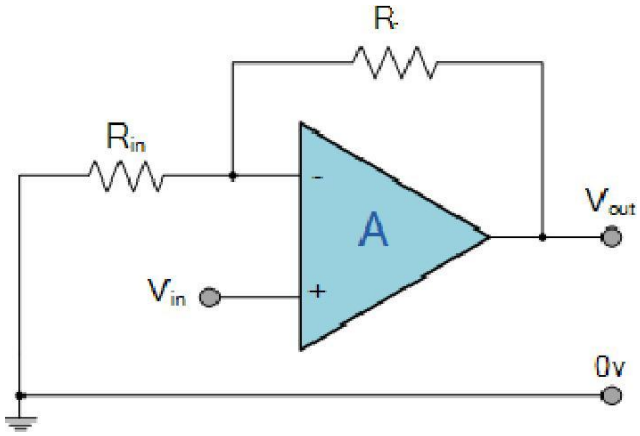
Then the closed loop voltage gain of a **Non-inverting Operational Amplifier** will be given as:

$$A_{(V)} = 1 + \frac{R_F}{R_2}$$

We can see from the equation above, that the overall closed-loop gain of a non-inverting amplifier will always be greater but never less than one (unity), it is positive in nature and is determined by the ratio of the values of Rf and R2.

If the value of the feedback resistor Rf is zero, the gain of the amplifier will be exactly equal to one (unity). If resistor R2 is zero the gain will approach infinity, but in practice it will be limited to the operational amplifiers open-loop differential gain, (Ao).

We can easily convert an inverting operational amplifier configuration into a non-inverting amplifier configuration by simply changing the input connections as shown.



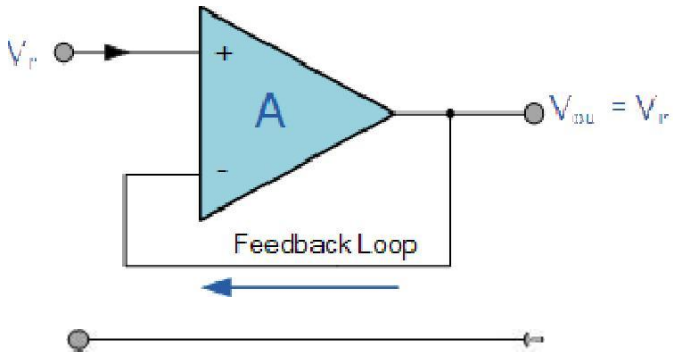
Voltage Follower (Unity Gain Buffer)

If we made the feedback resistor, Rf equal to zero, (Rf = 0), and resistor R2 equal to infinity, (R2 =), then the circuit would have a fixed gain of "1" as all the output voltage would be present on the inverting input terminal (negative feedback). This would then produce a special type of the non-inverting amplifier circuit called a **Voltage Follower** or also called a "unity gain buffer".

As the input signal is connected directly to the non-inverting input of the amplifier the output signal is not inverted resulting in the output voltage being equal to the input voltage, Vout = Vin. This then makes the **voltage follower** circuit ideal as a Unity Gain Buffer circuit because of its isolation properties.

The advantage of the unity gain voltage follower is that it can be used when impedance matching or circuit isolation is more important than amplification as it maintains the signal voltage. The input impedance of the voltage follower circuit is very high, typically above 1M as it is equal to that of the operational amplifiers input resistance times its gain (Rin x Ao). Also its output impedance is very low since an ideal op-amp condition is assumed.

Non-inverting Voltage Follower



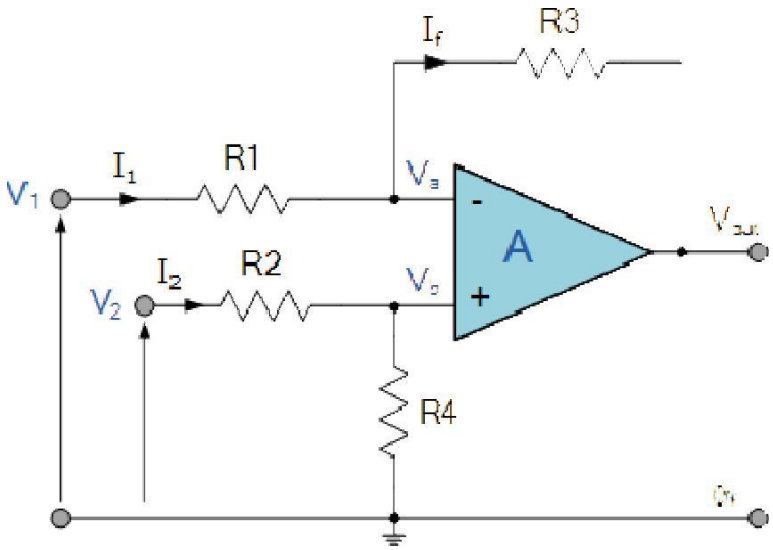
In this non-inverting circuit configuration, the input impedance Rin has increased to infinity and the feedback impedance R*f* reduced to zero. The output is connected directly back to the negative inverting input so the feedback is 100% and Vin is exactly equal to Vout giving it a fixed gain of 1 or unity. As the input voltage Vin is applied to the non-inverting input the gain of the amplifier is given as:

$$V_{out} = A(V_{in})$$

$$V_{in} = V+ \quad \text{and} \quad V_{out} = V-$$

$$\text{therefore Gain, } A_V = \frac{V_{out}}{V_{in}} = +$$

Differential Amplifier



By connecting each input in turn to 0v ground we can use superposition to solve for the output voltage Vout. Then the transfer function for a **Differential Amplifier** circuit is given as:

$$I_1 = \frac{V_2 - V_1}{R_1}, \quad I_2 = \frac{V - V_1}{R_2}, \quad I_3 = \frac{V_1 - (V_{out})}{R_3}$$

$$\text{Summing point } V_1 = V_1$$

$$\text{and} \quad V = V_2 \left(\frac{R_4}{R_3 + R_4} \right)$$

$$\text{If } V_2 = 0, \text{ then: } V_{out(1)} = -V_1 \left(\frac{R_3}{R_1} \right)$$

$$\text{If } V_1 = 0, \text{ then: } V_{out(2)} = V_2 \left(\frac{R_4}{R_3 + R_4} \right) \left(\frac{R_1 + R_3}{R_1} \right)$$

$$V_{out} = V_{out(1)} + V_{out(2)}$$

$$\therefore V_{out} = -V_1 \left(\frac{R_3}{R_1} \right) + V \left(\frac{R_4}{R_3 + R_4} \right) \left(\frac{R_1 + R_3}{R_1} \right)$$

When resistors, R1 = R2 and R3 = R4 the above transfer function for the differential amplifier can be simplified to the following expression:

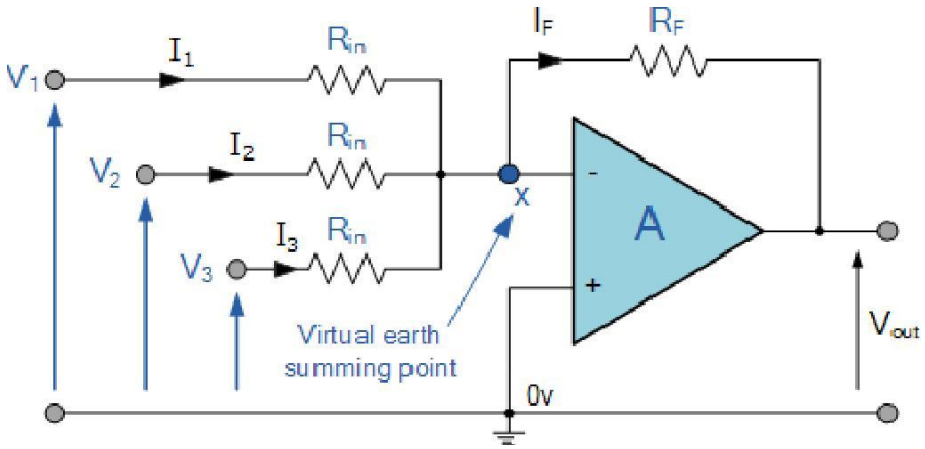
Differential Amplifier Equation

$$V_{OUT} = \frac{R_3}{R_1} (V_2 - V_1)$$

If all the resistors are all of the same ohmic value, that is: R1 = R2 = R3 = R4 then the circuit will become a **Unity Gain Differential Amplifier** and the voltage gain of the amplifier will be exactly one or unity. Then the output expression would simply be Vout = V2 - V1. Also note that if input V1 is higher than input V2 the output voltage sum will be negative, and if V2 is higher than V1, the output voltage sum will be positive.

The **Differential Amplifier** circuit is a very useful op-amp circuit and by adding more resistors in parallel with the input resistors R1 and R3, the resultant circuit can be made to either “Add” or “Subtract” the voltages applied to their respective inputs. One of the most common ways of doing this is to connect a “Resistive Bridge” commonly called a *Wheatstone Bridge* to the input of the amplifier as shown below.

Summing Amplifier Circuit



The output voltage, (Vout) now becomes proportional to the sum of the input voltages, V1, V2, V3 etc. Then we can modify the original equation for the inverting amplifier to take account of these new inputs thus:

$$I_F = I_1 + I_2 + I_3 = -\left[\frac{V_1}{R_{in}} + \frac{V_2}{R_{in}} + \frac{V_3}{R_{in}}\right]$$

$$\text{Inverting Equation: } V_{out} = -\frac{R_f}{R_{in}} \times V_{in}$$

$$\text{then, } -V_{out} = \left[\frac{R_F}{R_{in}}V_1 + \frac{R_F}{R_{in}}V_2 + \frac{R_F}{R_{in}}V_3\right]$$

However, if all the input impedances, (Rin) are equal in value, we can simplify the above equation to give an output voltage of:

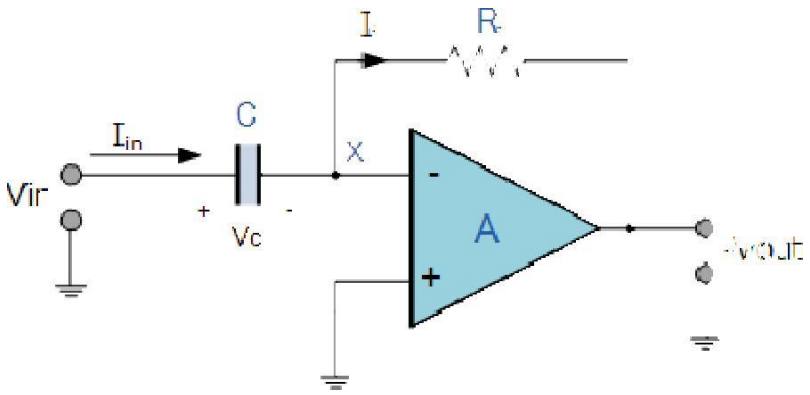
Summing Amplifier Equation

$$-V_{out} = \frac{R_F}{R_{IN}}\left(V_1 + V_2 + V_3 \ldots \text{etc}\right)$$

We now have an operational amplifier circuit that will amplify each individual input voltage and produce an output voltage signal that is proportional to the algebraic “SUM” of the three individual input voltages V_1, V_2 and V_3. We can also add more inputs if required as each individual input “see’s” their respective resistance, Rin as the only input impedance.

This is because the input signals are effectively isolated from each other by the “virtual earth” node at the inverting input of the op-amp. A direct voltage addition can also be obtained when all the resistances are of equal value and Rf is equal to Rin.

Op-amp Differentiator Circuit



The input signal to the differentiator is applied to the capacitor. The capacitor blocks any DC content so there is no current flow to the amplifier summing point, X resulting in zero output voltage. The capacitor only allows AC type input voltage changes to pass through and whose frequency is dependant on the rate of change of the input signal.

At low frequencies the reactance of the capacitor is “High” resulting in a low gain (Rf/Xc) and low output voltage from the op-amp. At higher frequencies the reactance of the capacitor is much lower resulting in a higher gain and higher output voltage from the differentiator amplifier.

However, at high frequencies an op-amp differentiator circuit becomes unstable and will start to oscillate. This is due mainly to the first-order effect, which determines the frequency response of the op-amp circuit causing a second-order response which, at high frequencies gives an output voltage far higher than what would be expected. To avoid this the high frequency gain of the circuit needs to be reduced by adding an additional small value capacitor across the feedback resistor Rf.

Ok, some math’s to explain what’s going on!. Since the node voltage of the operational amplifier at its inverting input terminal is zero, the current, i flowing through the capacitor will be given as:

$$I_{IN} = I_F = -\frac{V_{OUT}}{R_F}$$

The charge on the capacitor equals Capacitance x Voltage across the capacitor

$$Q = C \times V_{IN}$$

The rate of change of this charge is

$$\frac{dQ}{dt} = C\frac{dV_{IN}}{dt}$$

but dQ/dt is the capacitor current i

$$i_{IN} = C\frac{dV_{IN}}{dt} = i_F$$

$$\therefore -\frac{V_{OUT}}{R_F} = C\frac{dV_{IN}}{dt}$$

from which we have an ideal voltage output for the op-amp differentiator is given as:

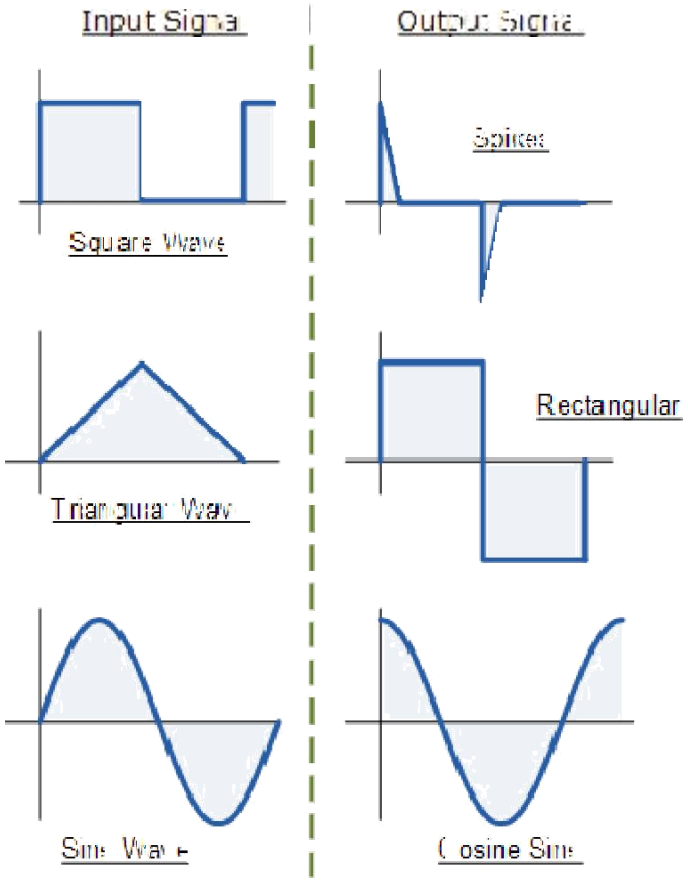
$$V_{OUT} = -R_F C\frac{dV_{IN}}{dt}$$

Therefore, the output voltage Vout is a constant -Rf.C times the derivative of the input voltage Vin with respect to time. The minus sign indicates a 180^{o} phase shift because the input signal is connected to the inverting input terminal of the operational amplifier.

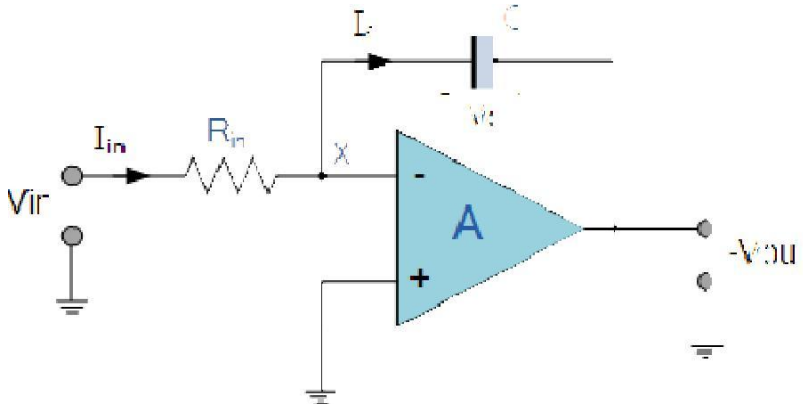
One final point to mention, the **Op-amp Differentiator** circuit in its basic form has two main disadvantages compared to the previous Operational Amplifier Integrator circuit. One is that it suffers from instability at high frequencies as mentioned above, and the other is that the capacitive input makes it very susceptible to random noise signals and any noise or harmonics present in the source circuit will be amplified more than the input signal itself. This is because the output is proportional to the slope of the input voltage so some means of limiting the bandwidth in order to achieve closed-loop stability is required

Op-amp Differentiator Waveforms

If we apply a constantly changing signal such as a Square-wave, Triangular or Sine-wave type signal to the input of a differentiator amplifier circuit the resultant output signal will be changed and whose final shape is dependant upon the RC time constant of the Resistor/Capacitor combination.



Op-amp Integrator Circuit



As its name implies, the **Op-amp Integrator** is an Operational Amplifier circuit that performs the mathematical operation of **Integration**, that is we can cause the output to respond to changes in the input voltage over time as the op-amp integrator produces an *output voltage which is proportional to the integral of the input voltage*.

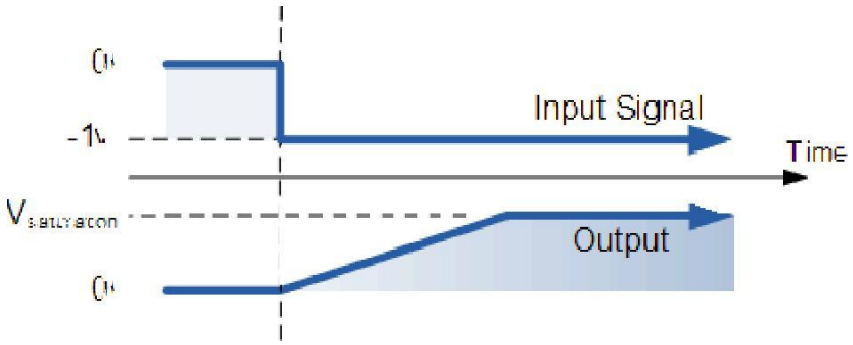
In other words the magnitude of the output signal is determined by the length of time a voltage is present at its input as the current through the feedback loop charges or discharges the capacitor as the required negative feedback occurs through the capacitor.

When a step voltage, Vin is firstly applied to the input of an integrating amplifier, the uncharged capacitor C has very little resistance and acts a bit like a short circuit allowing maximum current to flow via the input resistor, Rin as potential difference exists between the two plates. No current flows into the amplifiers input and point X is a virtual earth resulting in zero output. As the impedance of the capacitor at this point is very low, the gain ratio of Xc/Rin is also very small giving an overall voltage gain of less than one, (voltage follower circuit).

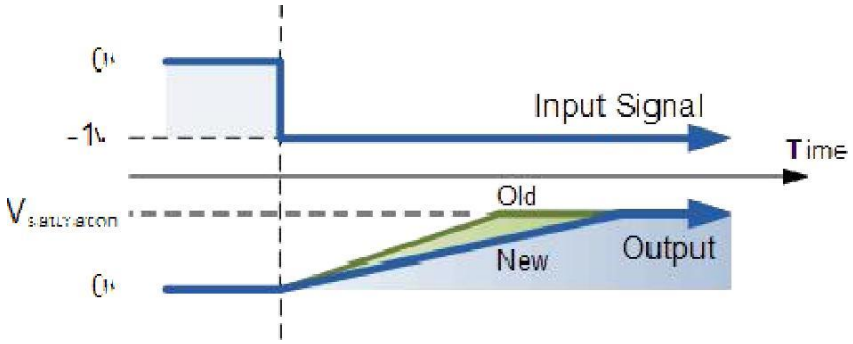
As the feedback capacitor, C begins to charge up due to the influence of the input voltage, its impedance Xc slowly increase in proportion to its rate of charge. The capacitor charges up at a rate determined by the RC time constant, ( ) of the series RC network. Negative feedback forces the op-amp to produce an output voltage that maintains a virtual earth at the op-amp's inverting input.

Since the capacitor is connected between the op-amp's inverting input (which is at earth potential) and the op-amp's output (which is negative), the potential voltage, Vc developed across the capacitor slowly increases causing the charging current to decrease as the impedance of the capacitor increases. This results in the ratio of Xc/Rin increasing producing a linearly increasing ramp output voltage that continues to increase until the capacitor is fully charged.

At this point the capacitor acts as an open circuit, blocking any more flow of DC current. The ratio of feedback capacitor to input resistor (Xc/Rin) is now infinite resulting in infinite gain. The result of this high gain (similar to the op-amps open-loop gain), is that the output of the amplifier goes into saturation as shown below. (Saturation occurs when the output voltage of the amplifier swings heavily to one voltage supply rail or the other with little or no control in between).

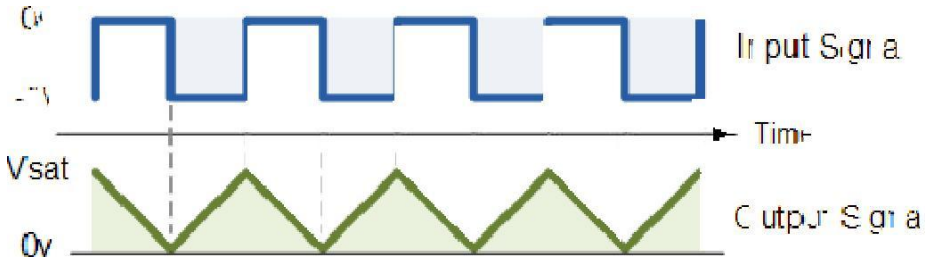


The rate at which the output voltage increases (the rate of change) is determined by the value of the resistor and the capacitor, “RC time constant“. By changing this RC time constant value, either by changing the value of the Capacitor, C or the Resistor, R, the time in which it takes the output voltage to reach saturation can also be changed for example.



If we apply a constantly changing input signal such as a square wave to the input of an **Integrator Amplifier** then the capacitor will charge and discharge in response to changes in the input signal. This results in the output signal being that of a sawtooth waveform whose frequency is dependant upon the RC time constant of the resistor/capacitor combination. This type of circuit is also known as a **Ramp Generator** and the transfer function is given below.

Op-amp Integrator Ramp Generator



We know from first principals that the voltage on the plates of a capacitor is equal to the charge on the capacitor divided by its capacitance giving Q/C. Then the voltage across the capacitor is output Vout therefore: -Vout = Q/C. If the capacitor is charging and discharging, the rate of charge of voltage across the capacitor is given as:

$$V_C = \frac{Q}{C} \qquad V_C = V_X - V_{out} = 0 - V_{out}$$

$$\therefore -\frac{dV_{out}}{dt} = \frac{dQ}{C\,dt} = \frac{1}{C}\frac{dQ}{dt}$$

But dQ/dt is electric current and since the node voltage of the integrating op-amp at its inverting input terminal is zero, X = 0, the input current I(in) flowing through the input resistor, Rin is given as:

$$i_{in} = \frac{V_{in} - 0}{R_{in}} = \frac{V_{in}}{R_{in}}$$

The current flowing through the feedback capacitor C is given as:

$$i_f = C\frac{dV_{out}}{dt} = C\frac{dQ}{C\,dt} = \frac{dQ}{dt} = C\frac{dV_{out}}{dt}$$

Assuming that the input impedance of the op-amp is infinite (ideal op-amp), no current flows into the op-amp terminal. Therefore, the nodal equation at the inverting input terminal is given as:

$$i_{in} = i_f = \frac{V_{in}}{R_{in}} = C\frac{dV_{out}}{dt}$$

$$\therefore \frac{V_{in}}{V_{out}} \times \frac{dt}{R_{in}C} = 1$$

From which we derive an ideal voltage output for the **Op-amp Integrator** as:

$$V_{out} = -\frac{1}{R_{in} C}\int_0^t V_{in}\, dt = -\int_0^t V_{in}\, \frac{dt}{R_{in} C}$$

To simplify the math's a little, this can also be re-written as:

$$V_{out} = -\frac{1}{\omega RC} V_{in}$$

Where = 2 f and the output voltage Vout is a constant 1/RC times the integral of the input voltage Vin with respect to time. The minus sign (-) indicates a 180^{o} phase shift because the input signal is connected directly to the inverting input terminal of the op-amp.

Amplifier classes:-

Generally, large signal or Power Amplifiers are used in the output stages of audio amplifier systems to drive a loudspeaker load. A typical loudspeaker has an impedance of between 4 and , thus a power amplifier must be able to supply the high peak currents required to drive the low impedance speaker.

One method used to distinguish the electrical characteristics of different types of amplifiers is by "class", and as such amplifiers are classified according to their circuit configuration and method of operation. Then **Amplifier Classes** is the term used to differentiate between the different amplifier types.

Amplifier Classes represent the amount of the output signal which varies within the amplifier circuit over one cycle of operation when excited by a sinusoidal input signal. The classification of amplifiers range from entirely linear operation (for use in high-fidelity signal amplification) with very low efficiency, to entirely non-linear (where a faithful signal reproduction is not so important) operation but with a much higher efficiency, while others are a compromise between the two.

Amplifier classes are mainly lumped into two basic groups. The first are the classically controlled conduction angle amplifiers forming the more common amplifier classes of A, B, AB and C, which are defined by the length of their conduction state over some portion of the output waveform, such that the output stage transistor operation lies somewhere between being "fully-ON" and "fully-OFF".

The second set of amplifiers are the newer so-called "switching" amplifier classes of D, E, F, G, S, T etc, which use digital circuits and pulse width modulation (PWM) to constantly switch the

signal between “fully-ON” and “fully-OFF” driving the output hard into the transistors saturation and cut-off regions.

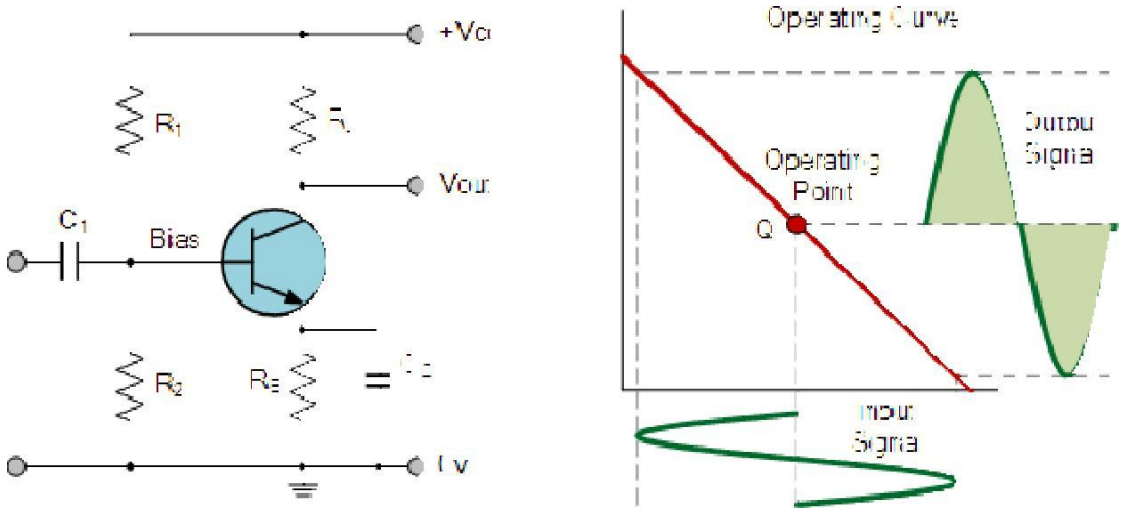
The most commonly constructed amplifier classes are those that are used as audio amplifiers, mainly class A, B, AB and C and to keep things simple, it is these types of **amplifier classes** we will look at here in more detail.

Class A Amplifier

Class A Amplifiers are the most common type of amplifier class due mainly to their simple design. Class A, literally means “the best class” of amplifier due mainly to their low signal distortion levels and are probably the best sounding of all the amplifier classes mentioned here. The class A amplifier has the highest linearity over the other amplifier classes and as such operates in the linear portion of the characteristics curve.

Generally class A amplifiers use the same single transistor (Bipolar, FET, IGBT, etc) connected in a common emitter configuration for both halves of the waveform with the transistor always having current flowing through it, even if it has no base signal. This means that the output stage whether using a Bipolar, MOSFET or IGBT device, is never driven fully into its cut-off or saturation regions but instead has a base biasing Q-point in the middle of its load line. Then the transistor never turns “OFF” which is one of its main disadvantages.

Class A Amplifier



To achieve high linearity and gain, the output stage of a class A amplifier is biased “ON” (conducting) all the time. Then for an amplifier to be classified as “Class A” the zero signal idle current in the output stage must be equal to or greater than the maximum load current (usually a loudspeaker) required to produce the largest output signal.

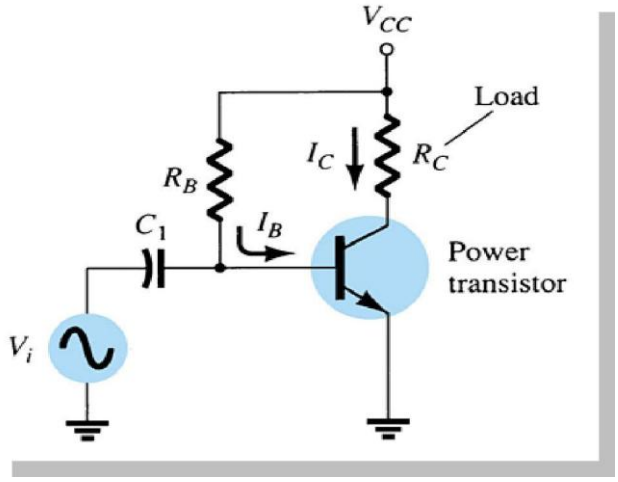
As a class A amplifier operates in the linear portion of its characteristic curves, the single output device conducts through a full 360 degrees of the output waveform. Then the class A amplifier is equivalent to a current source.

Since a class A amplifier operates in the linear region, the transistors base (or gate) DC biasing voltage should by chosen properly to ensure correct operation and low distortion. However, as the output device is “ON” at all times, it is constantly carrying current, which represents a continuous loss of power in the amplifier.

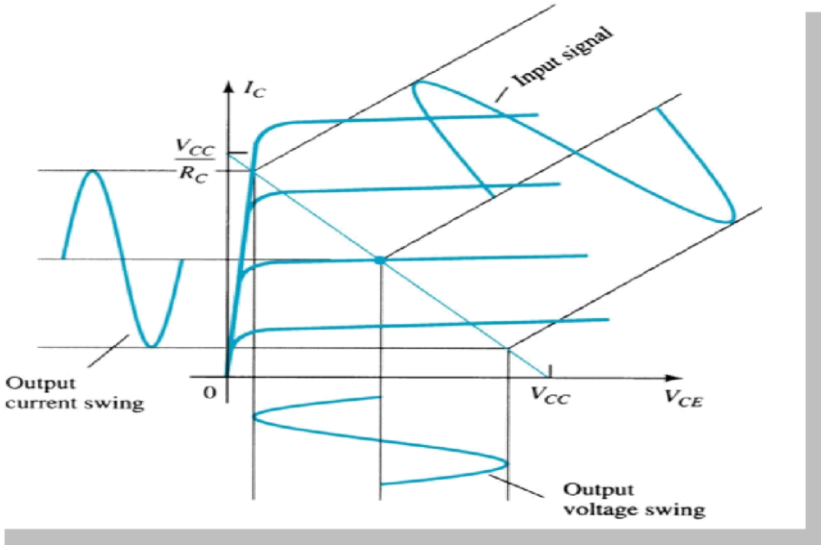
Due to this continuous loss of power class A amplifiers create tremendous amounts of heat adding to their very low efficiency at around 30%, making them impractical for high-power amplifications. Also due to the high idling current of the amplifier, the power supply must be sized accordingly and be well filtered to avoid any amplifier hum and noise. Therefore, due to the low efficiency and over heating problems of Class A amplifiers, more efficient amplifier classes have been developed.

Series-Fed Class A Amplifier

This is similar to the small-signal amplifier except that it will handle higher voltages. The transistor used is a high-power transistor.



When an input signal is applied the output will vary from its dc bias operating voltage and current. A small input signal causes the output voltage to swing to a maximum of V_{cc} and a minimum of 0V. The current can also swing from 0mA to I_{CSAT} (V_{CC}/R_C).



Input power:

The power into the amplifier is from the DC supply. With no input signal, the DC current drawn is the collector bias current, I_{CQ}.

$$P_{i(dc)} = V_{CC} I_{CQ}$$

Output Power

$$P_{o(ac)} = \frac{V_{C(rms)}^2}{R_C}$$

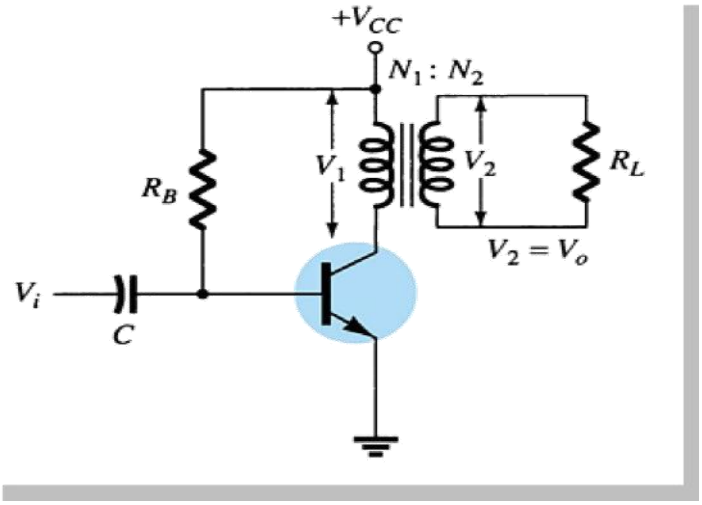
$$P_{o(ac)} = V_{C(rms)} I_{C(rms)}$$

Efficiency

$$\frac{P_{o(ac)}}{P_{i(ac)}} 100$$

Transformer-Coupled Class A Amplifier:

This circuit uses a transformer to couple to the load. This improves the efficiency of the Class A to 50%.

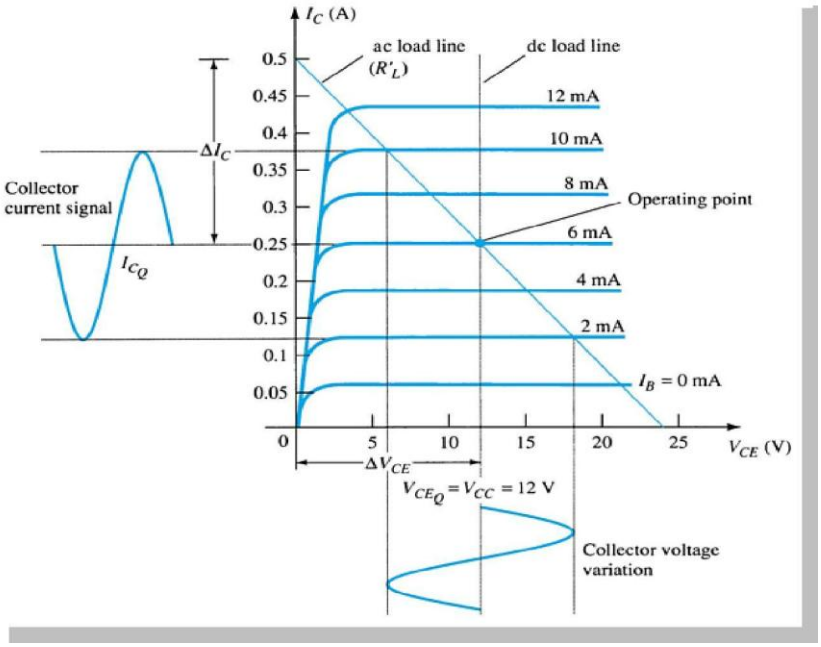


DC Load Line

As in all class A amplifiers the Q-point is established close to the midpoint of the DC load line. The dc resistance is small ideally at 0 and a dc load line is a straight vertical line.

AC Load Line

The saturation point (I_{Cmax}) is at V_{cc}/R_L and the cutoff point is at V_2 (the secondary voltage of the transformer). This increases the maximum output swing because the minimum and maximum values of I_C and V_{CE} are spread further apart.



Signal Swing and Output AC Power

The voltage swing:

$$V_{CE(pp)} \quad V_{CE\,max} \quad V_{CE\,min}$$

The current swing:

$$I_{c(pp)} \quad I_{C\,max} \quad I_{C\,min}$$

The AC power:

$$P_{o(ac)} \quad \frac{(V_{CEmax} \quad V_{CEmin})(I_{Cmax} \quad I_{Cmin})}{8} \quad (\text{max } imum)$$

Power input from the DC source:

$$P_{i(dc)} \quad V_{CC}\ I_{CQ}$$

Power dissipated as heat across the transistor:

$$P_{Q} \quad P_{i(dc)} \quad P_{o(ac)}$$

Maximum efficiency:

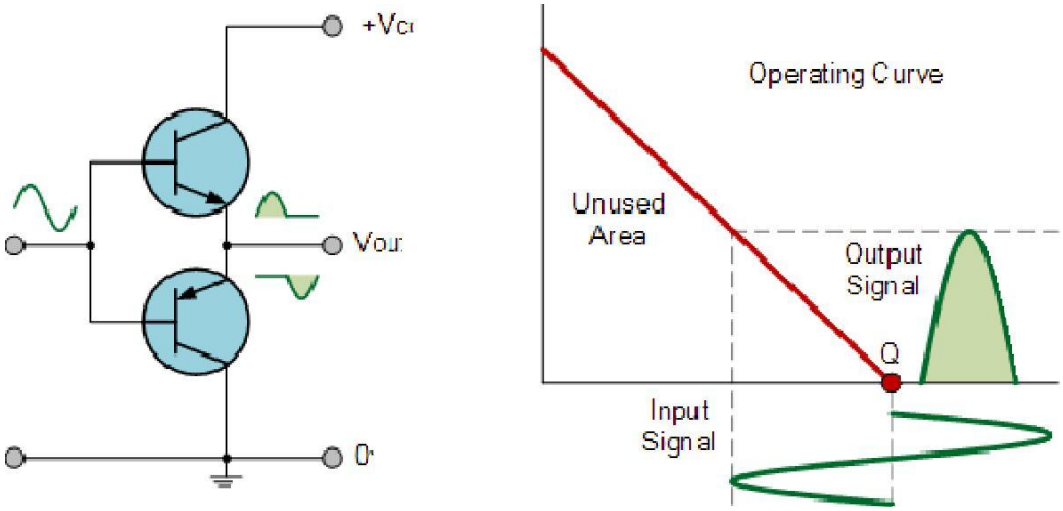
$$50 \quad \frac{V_{CEmax} \quad \text{[illegible]}^2}{V_{CEmax} \quad V_{CEmin}}$$

Class B Amplifier

Class B amplifiers were invented as a solution to the efficiency and heating problems associated with the previous class A amplifier. The basic class B amplifier uses two complimentary transistors either bipolar of FET for each half of the waveform with its output stage configured in a “push-pull” type arrangement, so that each transistor device amplifies only half of the output waveform.

In the class B amplifier, there is no DC base bias current as its quiescent current is zero, so that the dc power is small and therefore its efficiency is much higher than that of the class A amplifier. However, the price paid for the improvement in the efficiency is in the linearity of the switching device.

Class B Amplifier



When the input signal goes positive, the positive biased transistor conducts while the negative transistor is switched “OFF”. Likewise, when the input signal goes negative, the positive transistor switches “OFF” while the negative biased transistor turns “ON” and conducts the negative portion of the signal. Thus the transistor conducts only half of the time, either on positive or negative half cycle of the input signal.

Then we can see that each transistor device of the class B amplifier only conducts through one half or 180 degrees of the output waveform in strict time alternation, but as the output stage has devices for both halves of the signal waveform the two halves are combined together to produce the full linear output waveform.

This push-pull design of amplifier is obviously more efficient than Class A, at about 50%, but the problem with the class B amplifier design is that it can create distortion at the zero-crossing point of the waveform due to the transistors dead band of input base voltages from -0.7V to +0.7.

We remember from the Transistor tutorial that it takes a base-emitter voltage of about 0.7 volts to get a bipolar transistor to start conducting. Then in a class B amplifier, the output transistor is not “biased” to an “ON” state of operation until this voltage is exceeded.

This means that the the part of the waveform which falls within this 0.7 volt window will not be reproduced accurately making the class B amplifier unsuitable for precision audio amplifier applications.

To overcome this zero-crossing distortion (also known as Crossover Distortion) class AB amplifiers were developed.

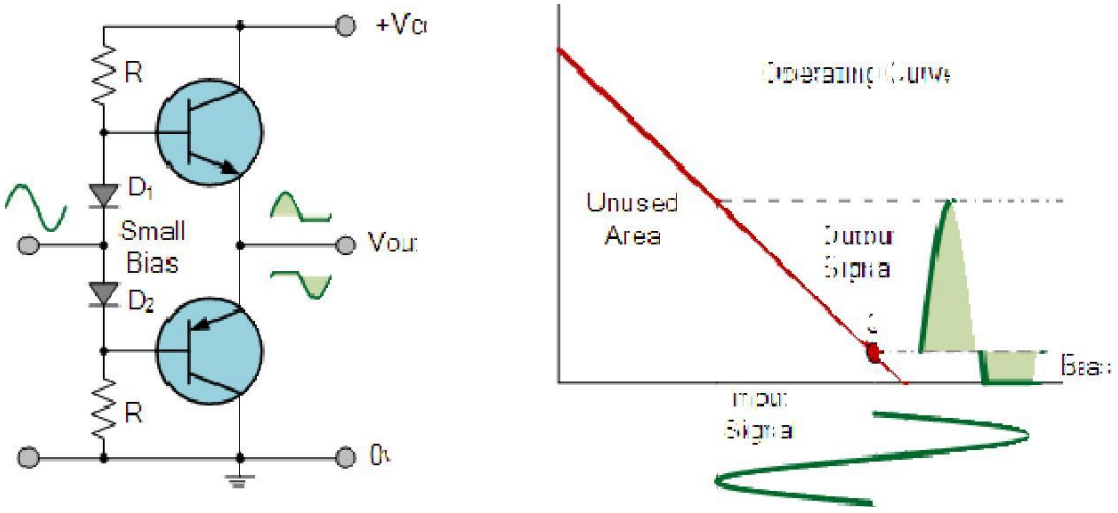
Class AB Amplifier

As its name suggests, the **Class AB Amplifier** is a combination of the “Class A” and the “Class B” type amplifiers we have looked at above. The AB classification of amplifier is currently one of the most common used types of audio power amplifier design. The class AB amplifier is a variation of a class B amplifier as described above, except that both devices are allowed to conduct at the same time around the waveforms crossover point eliminating the crossover distortion problems of the previous class B amplifier.

The two transistors have a very small bias voltage, typically at 5 to 10% of the quiescent current to bias the transistors just above its cut-off point. Then the conducting device, either bipolar of FET, will be “ON” for more than one half cycle, but much less than one full cycle of the input signal. Therefore, in a class AB amplifier design each of the push-pull transistors is conducting for slightly more than the half cycle of conduction in class B, but much less than the full cycle of conduction of class A.

In other words, the conduction angle of a class AB amplifier is somewhere between 180^{o} and 360^{o} depending upon the chosen bias point as shown.

Class AB Amplifier



The advantage of this small bias voltage, provided by series diodes or resistors, is that the crossover distortion created by the class B amplifier characteristics is overcome, without the inefficiencies of the class A amplifier design. So the class AB amplifier is a good compromise between class A and class B in terms of efficiency and linearity, with conversion efficiencies reaching about 50% to 60%.

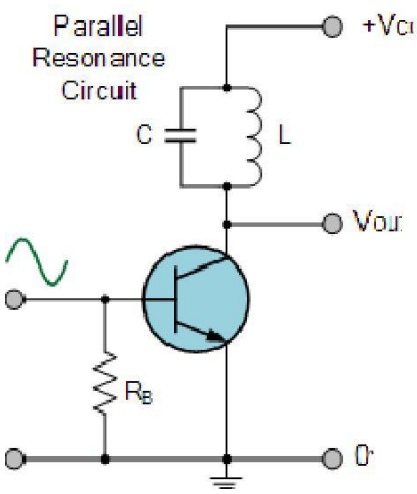
Class C Amplifier

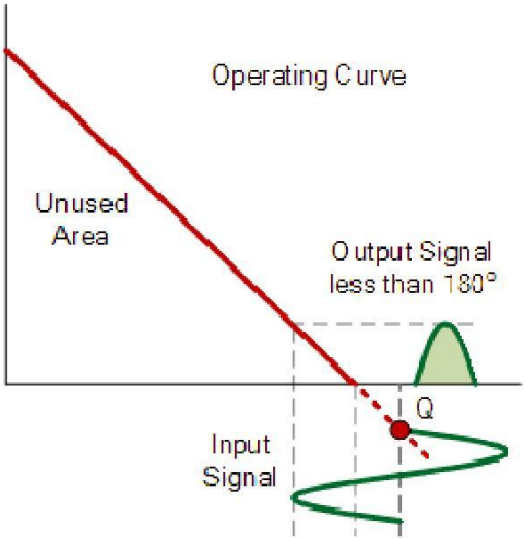
The **Class C Amplifier** design has the greatest efficiency but the poorest linearity of the classes of amplifiers mentioned here. The previous classes, A, B and AB are considered linear amplifiers, as the output signals amplitude and phase are linearly related to the input signals amplitude and phase.

However, the class C amplifier is heavily biased so that the output current is zero for more than one half of an input sinusoidal signal cycle with the transistor idling at its cut-off point. In other words, the conduction angle for the transistor is significantly less than 180 degrees, and is generally around the 90 degrees area.

While this form of transistor biasing gives a much improved efficiency of around 80% to the amplifier, it introduces a very heavy distortion of the output signal. Therefore, class C amplifiers are not suitable for use as audio amplifiers.

Class C Amplifier





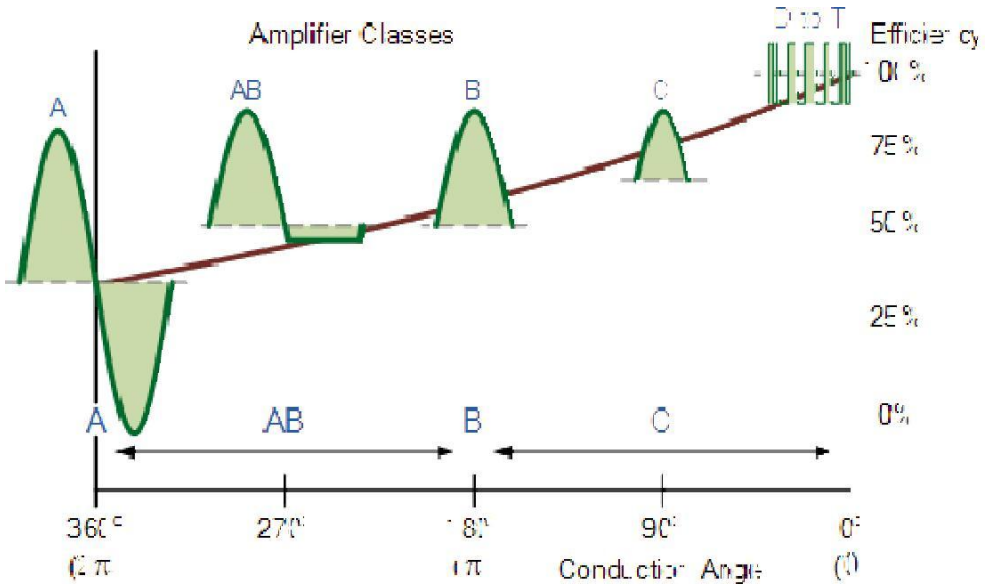
Due to its heavy audio distortion, class C amplifiers are commonly used in high frequency sine wave oscillators and certain types of radio frequency amplifiers, where the pulses of current produced at the amplifiers output can be converted to complete sine waves of a particular frequency by the use of LC resonant circuits in its collector circuit.

Amplifier Classes Summary

Then we have seen that the quiescent DC operating point (Q-point) of an amplifier determines the amplifier classification. By setting the position of the Q-point at half way on the load line of the amplifiers characteristics curve, the amplifier will operate as a class A amplifier. By moving the Q-point lower down the load line changes the amplifier into a class AB, B or C amplifier.

Then the class of operation of the amplifier with regards to its DC operating point can be given as:

Amplifier Classes and Efficiency



As well as audio amplifiers there are a number of high efficiency **Amplifier Classes** relating to switching amplifier designs that use different switching techniques to reduce power loss and increase efficiency. Some amplifier class designs listed below use RLC resonators or multiple power-supply voltages to reduce power loss, or are digital DSP (digital signal processing) type amplifiers which use pulse width modulation (PWM) switching techniques.

Feedback amplifier

Feedback is one of the fundamental processes in electronics. It is defined as the process whereby a portion of the output signal is fed to the input signal in order to form a part of the system-output control.

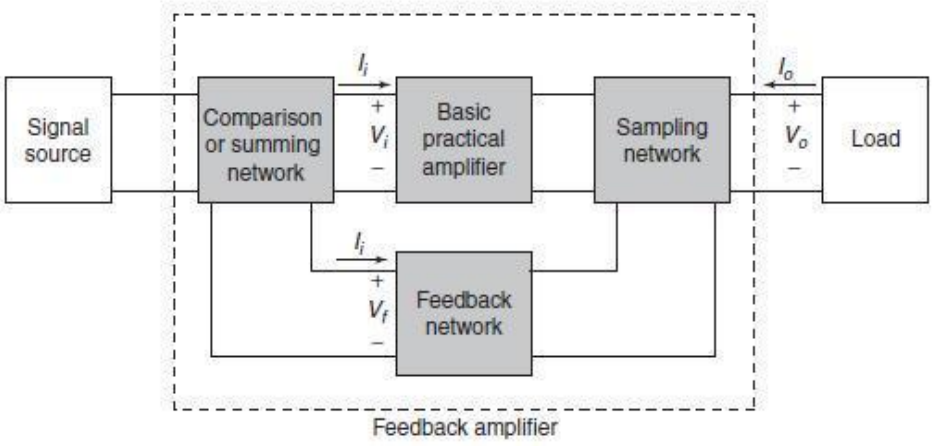
Feedback is used to make the operating point of a transistor insensitive to both manufacturing variations in *as well as temperature.*

There is another type of feedback called positive or regenerative feedback in which the overall gain of the amplifier is increased. Positive feedback is useful in oscillators and while establishing the two stable states of flip-flop.

The feedback system has many advantages especially in the control of impedance levels, bandwidth improvement, and in rendering the circuit performance relatively insensitive to manufacturing as well as to environmental changes.

These are the advantages of negative or degenerative feedback in which the signal feedback from output to input is 180 out of phase with the applied excitation. It increases bandwidth and input impedance, and lowers the output impedance.

Block diagram of a basic feedback amplifier



Block diagram of a basic feedback amplifier

Basic elements of feedback amplifier

Input Signal:

The signal source is modeled either by a voltage source Vs in series with a resistance Rs , or by a current source Is in parallel with a resistance Rs.

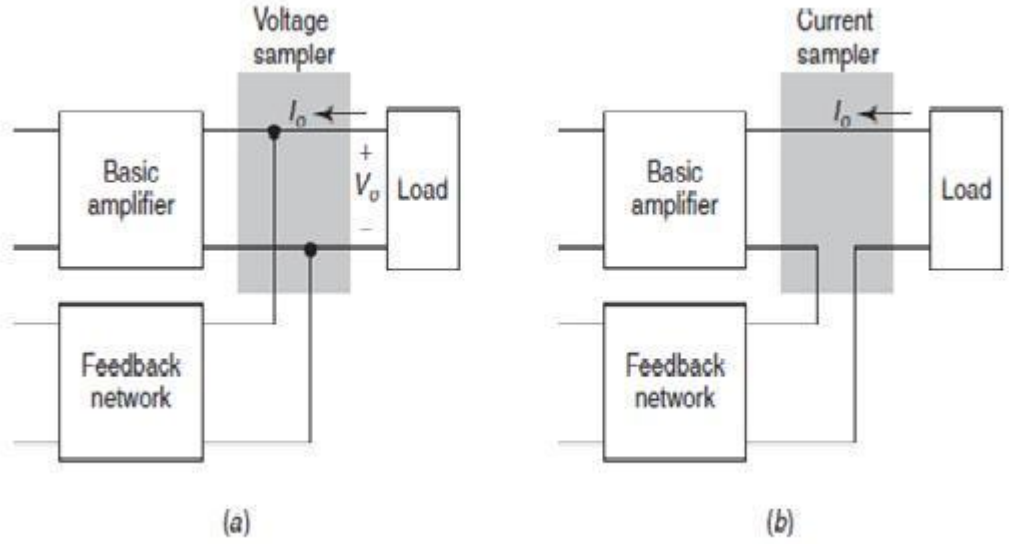
Output Signal:

The output can either be the voltage across the load resistance or the current through it. It is the output signal that is desired to be independent of the load and insensitive to parameter variations in the basic amplifier.

Sampling Network:

The function of the sampling network is to provide a measure of the output signal, i.e., a signal that is proportional to the output. This configuration is called shunt connection.

Measurement of the output voltage & current:



PROPERTIES OF NEGATIVE FEEDBACK:

Negative feedback has the following advantages:

- Negative feedback increases the input impedance of the voltage amplifier.
- The output impedance of the voltage amplifier can be further lowered by negative feedback.

The transfer gain *Af of the amplifier with a feedback can be stabilized against the variations of h or* hybrid parameters of the transistors, or the parameters of the other active devices used in the amplifier.

Negative feedback increases the frequency response and the bandwidth of the amplifier.

Negative feedback increases the linear range of operation of the amplifier.

Negative feedback causes reduction in noise.

Phase distortion is reduced.

Table 9-1 Signals and transfer ratios in feedback amplifiers

	Feedback Topology			
Signals	*Series-Shunt (Voltage-Series)*	*Series-Series (Current-Series)*	*Shunt-Series (Current-Shunt)*	*Shunt-Shunt (Voltage-Shunt)*
X_o	Voltage	Current	Current	Voltage
X_s, X_i, X_f	Voltage	Voltage	Current	Current
Ratio or Gain				
A	V_o/V_i	I_o/V_i	I_o/I_i	V_o/I_i
β	V_f/V_o	V_f/I_o	I_f/I_o	I_f/V_o
A_f	V_o/V_s	I_o/V_s	I_o/I_s	V_o/I_s

CALCULATIONS OF OPEN-LOOP GAIN, CLOSED-LOOP GAIN & FEEDBACK FACTORS:

The input signal *Xs , the output signal Xo , the feedback signal Xf and the difference signal Xi each represent* either a voltage or a current.

The symbol indicated by the circle with the summation sign enclosed within , represents the summing network whose output is the algebraic sum of inputs.

Thus, for a positive feedback, we get:

$$Xi = Xs + Xf$$

The signal *Xi , representing the output of the summing network is the amplifier input Xi . If the feedback* signal *Xf is 180 out of phase with the input Xs—as is true in negative feedback systems—then Xi is a difference*

signal. Therefore, *Xi decreases as* | *Xf* | *increases.*

The reverse transmission of the feedback network is defined by:

$$=Xf / Xa$$

The transfer function *is a real number, but in general it is a function of frequency. The gain of the basic* amplifier *A is defined as:*

$$A=Xo /Xi$$

Now, we get: $Xi =Xs / Xf$

Substituting the value of *Xf we get:*

$$Xi =Xs+ Xf = Xs+ Xo$$

we get:: $Xo= A*Xi$

Substituting the value of *Xi we get:*

$$Xo = A*Xi = A(Xs+ Xo) = AXs+A Xo$$

or, $Xo (1-A) = AXs$

Or, $Xo /X s=A/(1-A)$

The feedback gain *Af is obtained as:*

Af = Xo /Xs = A/(1-A)

we can represent the feedback gain as:

$$A_f = \frac{A}{1 \pm A\beta}$$

TOPOLOGIES OF THE FEEDBACK AMPLIFIER:

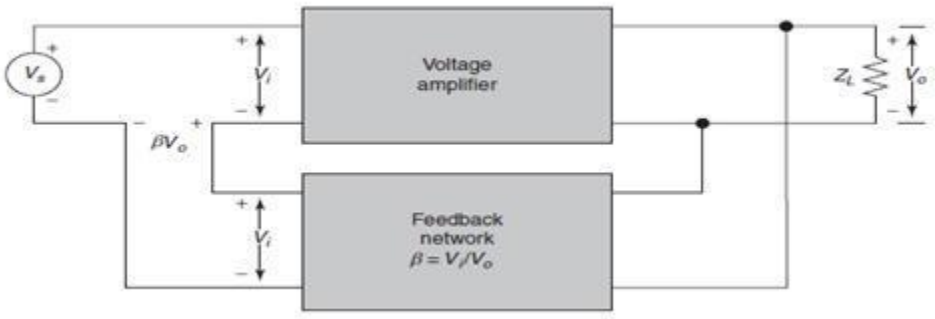
There are four basic amplifier types. Each of these is being approximated by the characteristics of an ideal controlled source. The four feedback topologies are as follows:

1. Series-shunt feedback
2. Series-series feedback
3. Shunt-series feedback
4. Shunt-shunt feedback

The alternative nomenclature used is as follows:

- Voltage-series or series-shunt feedback
- Current-series or series-series feedback
- Current-shunt or shunt-series feedback
- Voltage-shunt or shunt-shunt feedback

Voltage amplifiers with voltage-series feedback:



Voltage-series feedback:

Input Impedance with the feedback is:

$$Z_{if} = V_S / I_i$$

and $V_S = I_i Z_i + V_f = I_i Z_i + Vo$

Using voltage divider rule, we get:

$$Vo = A_V V_i Z_L / Z_0 + Z_L = A_V I_i Z_L$$

Where, $Ii = V_i / Z_0 + Z_L$

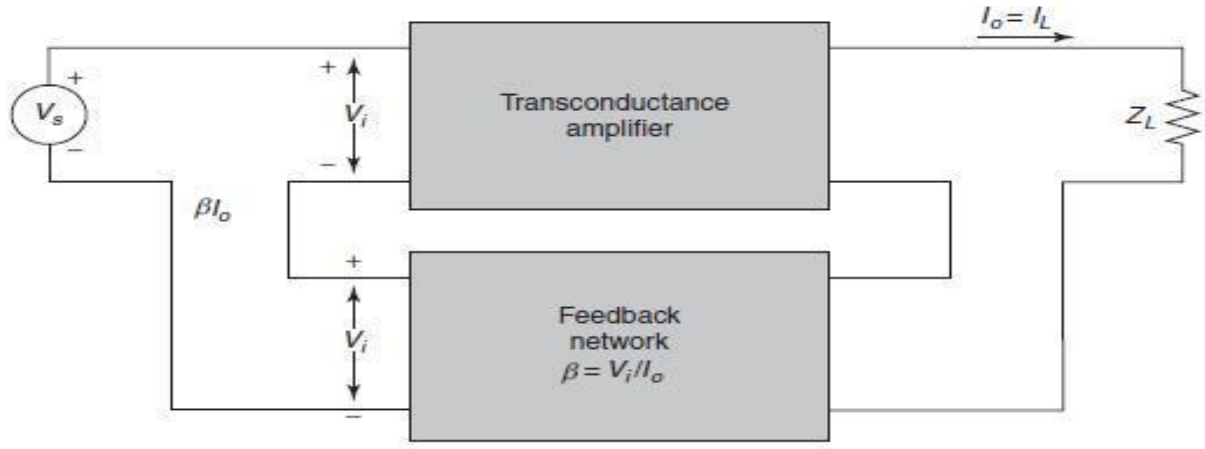
Now, $Vo = A_V I_i Z_L = A_V V_i$

Or $A_V = Vo / I_i$

The input impedance without feedback is:

$$Zi = Vi / Ii.$$

Current-Series or Series-Series Feedback:



Transconductance amplifier with current-series feedback

***Current-series feedback*:**

In a similar manner as for voltage series, for current series feedback we obtain:

$$Z_{if} = Z_i (1+ Y_M)$$

where, Y_M *is the short-circuit trans-admittance without feedback considering the load impedance, and is given by:*

$$Y_M = Io / V_i$$

$$Y_m Z_o /(Z_0 + Z_L)$$

where, Y_m *is the short-circuit trans-admittance without feedback.*

it is clear that for series mixing

$$Z if > Z i.$$

OSCILLATOR

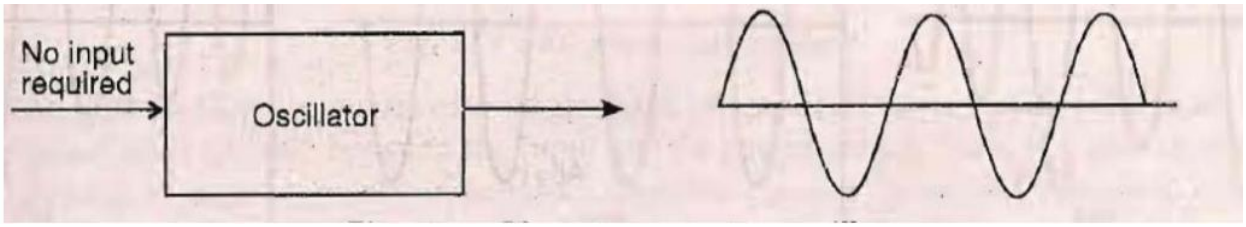
Oscillators: are the sources of sinusoidal electrical waves for electronic communication systems .

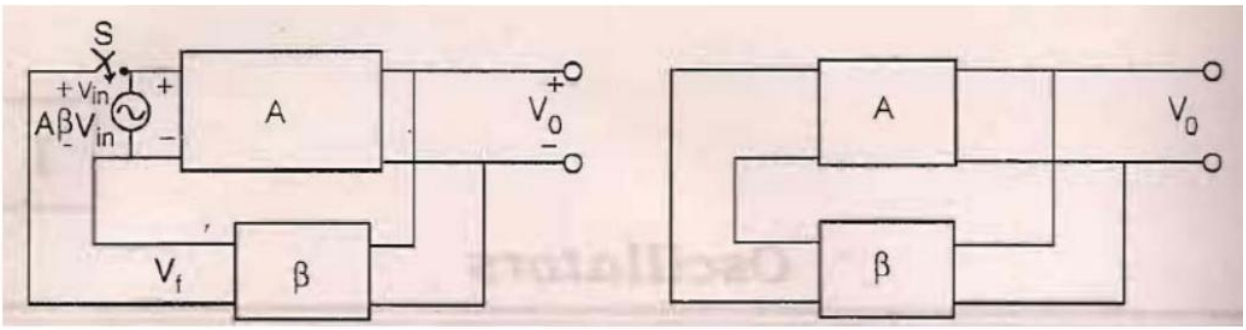
• They are supplied from a dcsource and they generate alternating voltages of high or low frequencies.

Operation of an Oscillator

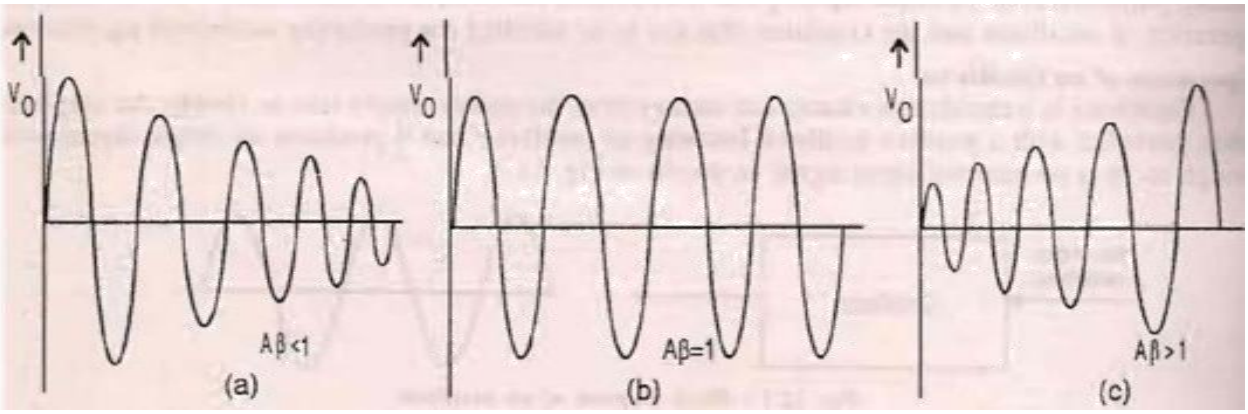
• Oscillator :is a circuit that changes dc energy from the power supply into ac energy.

• An amplifier provided with a positive feedbackbecomes an oscillator and it produces an output signal even thought there is no external input signal as shown.





A voltage sourceVin drives the input terminals of an amplifier. The amplifier output voltage is AVin and it drives the feedback network producing a feedback voltage Vf = A Vin . If the circuit of the amplifier and the feedback network provide correct phase shift, then this feedback voltage Vf will be in phase with signal Vin that drives the input terminals of the amplifier. Now, if switch is closed and simultaneously the voltage source Vin is removed, the feedback voltage Vf will drive the input terminals of the amplifier.



-If A is less than 1, A Vin will be less than Vin ,the signal feedback is not sufficient to drive the amplifier and the feedback circuits and the output will die out.

-If A >1, the output signal builds up resulting in oscillations with growing magnitude .

-If A =1, A Vin =Vin and the output voltage is a sine wave whose amplitude remains constant.

From the basic feedback equation

$$A_f = \frac{A}{1+\beta A}$$

• with A = -1and the term in the denominator becomes zero , then Af becomes infinite.

• Therefore, an infinitesimal signal (noise voltage) can produce an output signal even without an input signal and the circuit acts as an oscillator.

• The oscillations will not be sustained if, the magnitude of the product of the transfer gain amplifier and the magnitude of feedback factor of the feedback network is less than unity.

• The condition IA I = 1is called the Barkhausen criterion.

• It implies that when IA I =1, there exists an output voltage even in absence of any externally applied signal.

If IA I = 1precisely ,then after sometimes it is found that the A will either become lower or higher than unity .this due to change in the characteristics of active devices with voltage , temperature or ….

• Therefore, A is kept slightly larger than unity so that any variation in circuit parameters may not cause A to become less than unity otherwise the oscillation will stop.

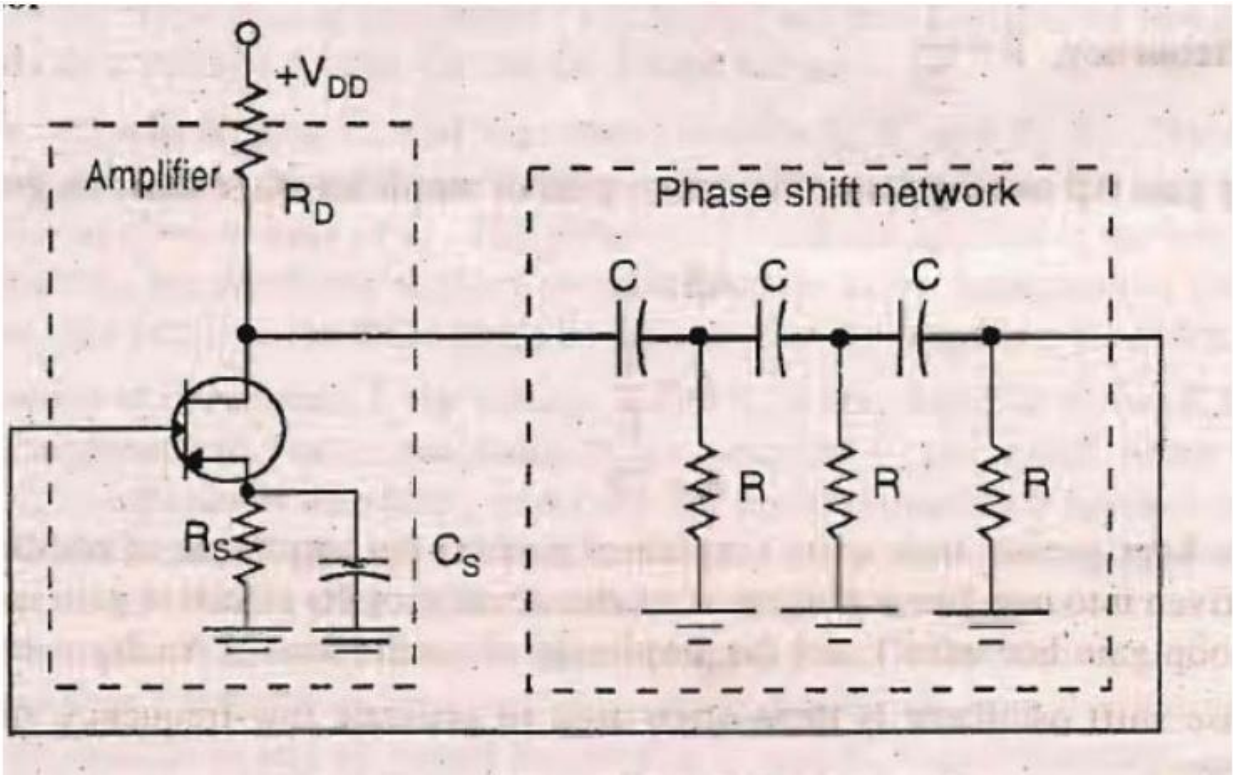
So, we can summarize the requirements of an oscillator circuit as:

• 1. Initially, the loop gain must be greater than unity at oscillator frequency.

• 2. After the desired output level is reached, A must decreaseto 1

• 3. At oscillator frequency, net phase shift around the loop must be zero or integer multiple of 360°so that the feedback signal is in phase with the starting infinitesimal voltage.

Phase Shift Oscillator:



A phase shift oscillatorconsists of a single stage of amplifier that amplifies the input signal and produces a phase shiftof 180°the input and its output signal.

• If a part of this output is taken and fed back to input, it results in negative feedbackcausing the output voltage to decrease.

• But we require positive feedbackwhich means that the voltage

• signal feedback should be in phase with the input signal.

• The output of the amplifier should taken through a phase-shift networkto provide it an additional phase shift of 180°.

• Amplifier provides a phase shift of 180°and the phase-shift network also gives a 180°and therefore, a total phase-shift of 360°(which is equivalent to 0°) results.

The RC network provides the required phase shift by using three RC

• Each having some value of R and C. these values are selected so as to produce 60°phase shift per section,resulting in total of 180°phase shift as desired .

• But in actual practice each RC-section does not provide the same phase shift because each section loads the previous one but the over all phase shift is 180°which is the requirement .

• The O/P of the phase shift network is connected to the I/P of the amplifier

.• The frequency at which phase shift is 180°is :

$$f = \frac{1}{2\pi RC\sqrt{6}}$$

This the frequency of oscillation

$$f = \frac{1}{2\pi RC\sqrt{6}}$$

At this frequency =1/29

• For loop gain A to be greater than unity,gain of amplifier stage

• must be greaterthan 29 ; A >1

=>A>1/

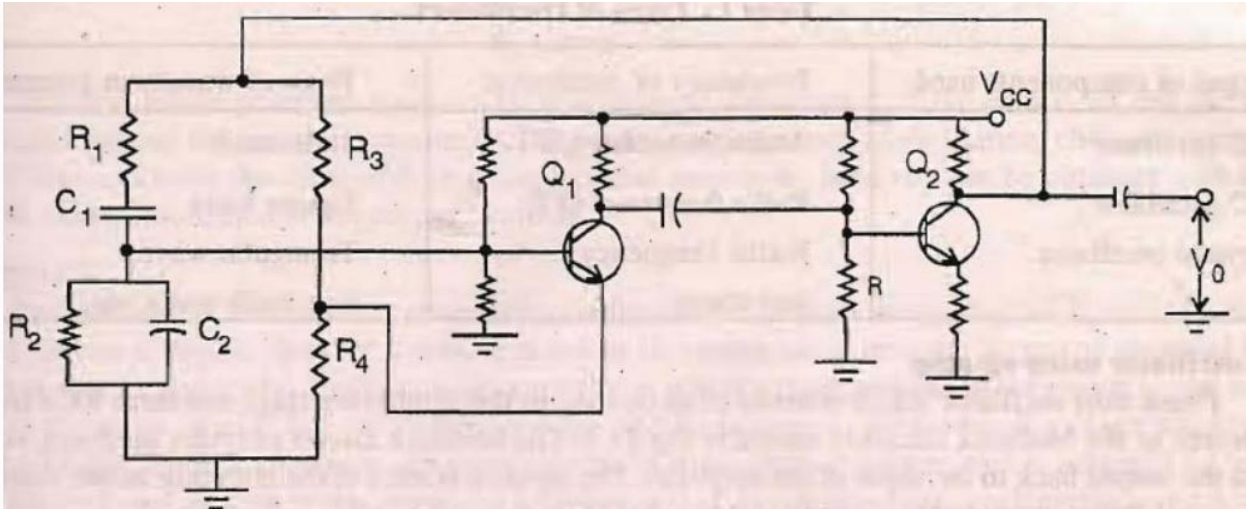
=>A>29.

Wein Bridge Oscillator

The principle

This type of oscillation uses two stages of amplifiers each providing a phase shift of 180.

The O/P of second stage is fed back to the I/P through a feed back network without producing any further phase shift .



WBO

 The wein bridge oscillator uses two stages to provide 180 phase shift per stageand a bridge network to control the frequency of oscillation.

 The bridge network consists of two parallel branches, each of which acts as a voltage divider for the feed-back voltage.

 One branch contains R3 and R4, and the other contains R1, C1, and R2, C2 •

 The feedback voltage developed across R4 of R3 R4 branch is applied to emitter of Q1, and the portion of voltage across R2 C2 of R1 C1,-R2 C2 branch is applied to base of Q1,.

 The polarity of feedback applied to the baseis such that it is regenerative (positive), and the feedback applied to emittertends to be degenerative (negative).

 For the circuit to oscillate, the positivefeedback must be greaterthan the negative feedback.

At the frequency of oscillation, fo, the voltage across R4is less than that across R2C2 • So, the circuit oscillates.

As the frequency increases, reactance of the capacitor C2decreases.

• Since C2shunts R2, the impedance of R2C2combination decreases, reducingthe positivefeedback applied to the base below the level of negative feedback applied to emitter.

• If the frequency tends to decrease, the reactance of C1increases causing more of the feedback voltage to be dropped across C1.

• This results in a corresponding decrease in positive feedbackdeveloped across R_2C_2. Hence, the positive feedback again becomes less than the negative feedback, preventing the circuit from oscillating.

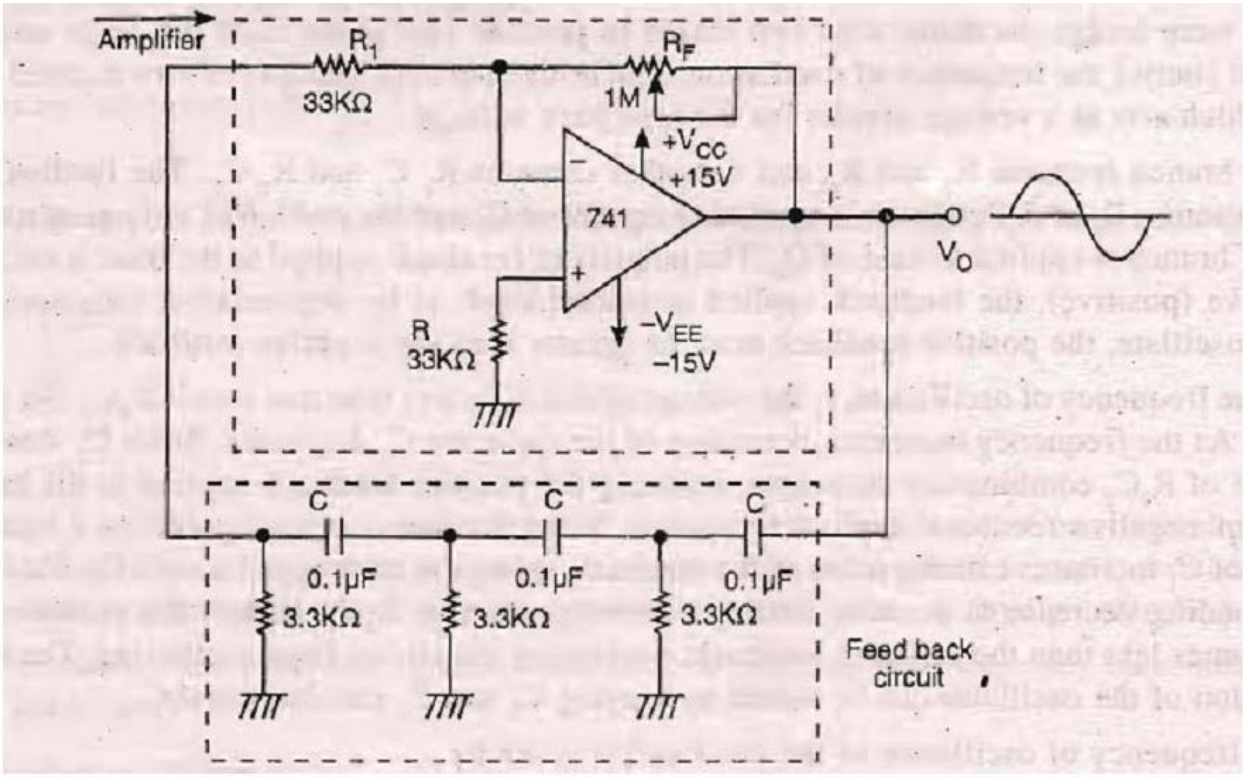
The frequency of oscillation of the oscillator can be varied by varying C1, and C2 simultaneously.

• The frequency of oscillation of the oscillator is given by :

$$f_o = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

RC oscillator using op-amp

Phase shift oscillator which consists of an op-amp as the amplifying stage and three RC cascade networks as the feedback circuit is shown.



RC oscillator using op-amp

• The feedback circuit provides feedback voltage from the output back to the input of the amplifier.

• The output of op-amp is shifted by 180°at the output. An additional 180°phase shift required for oscillation is provided by the cascaded RC networks.

• Thus the total phase shift around the loop is 360°.

• At some specific frequency when the phase shift of the cascaded RC networks is exactly 180°and the gain of the amplifier is sufficiently large, the circuit will oscillate at that frequency.

This frequency called the frequency of oscillation fo and is

$$f_o = \frac{1}{2\pi\sqrt{6}\,RC} = \frac{0.065}{RC}$$

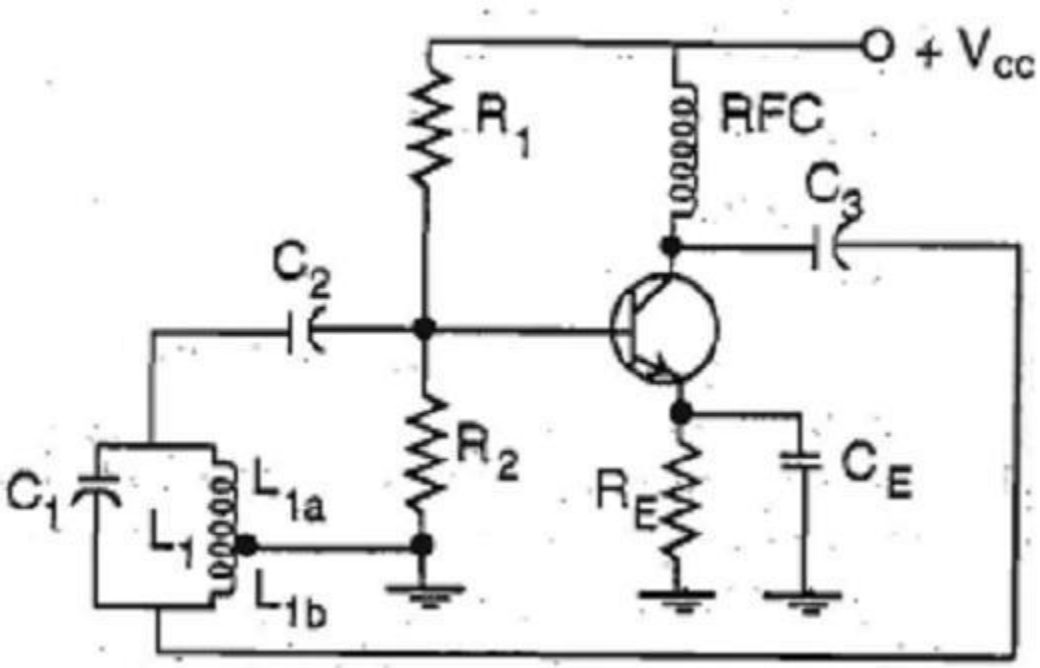
The circuit produces a sinusoidal waveform of frequency foif the gain is 29 and the total phase shift is exactly 360°.

• For a desired frequency of oscillation, choose a capacitor C, and then calculate the value of R.

Hartley Oscillator :-

This oscillator has two parts of coil .The first part is in the input circuit of cthe transistor and the other part is in the output circuit .The first part is used to supply ac voltage and the other part develops the positive feedback signal to sustain oscillation. The capacitor C1and the tapped coil L1 determine the frequency of the oscillator . The two sections of tapped coil are L1a and

L1b. L1ais in the base circuit and L1bis in the collector circuit of the transistor.



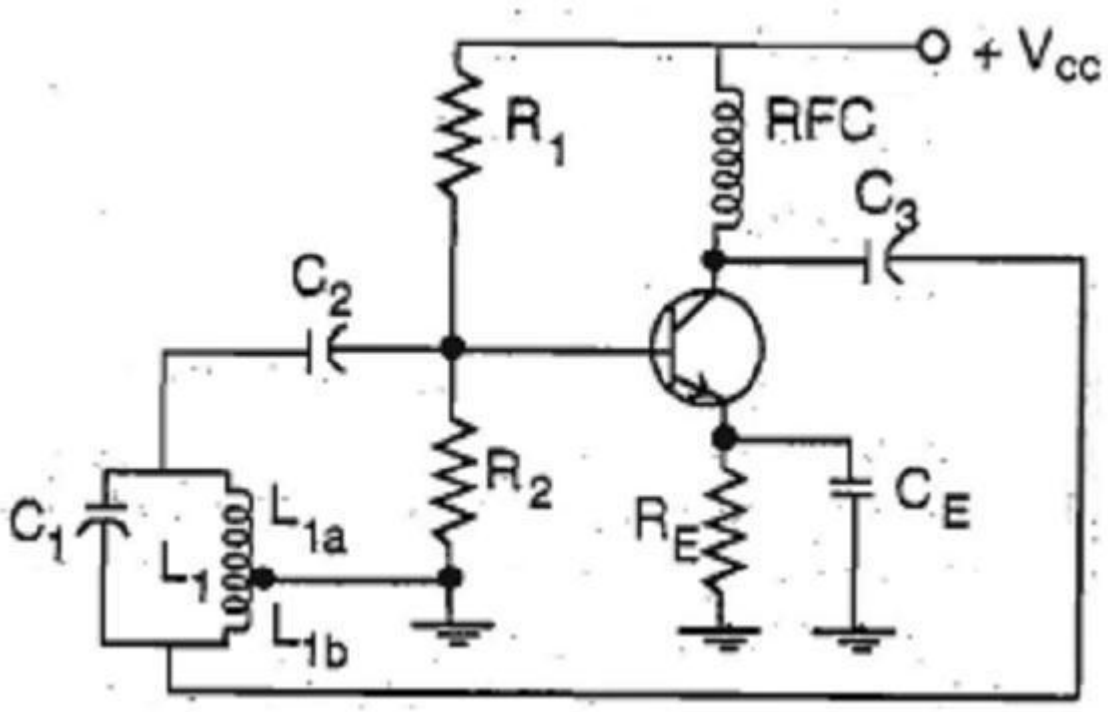
When V_{CC} is applied ,the collector current begins to flow. The drop in collector voltage is coupled through C_3 and developed across L_1b.

• This act as initial excitation for the tank causing a circulating current to flow in the tank.

• This circulating current induced voltage across L1awhich drives the base of the transistor.

• The amplified signal at the collector is coupled back to the tank circuit by C3and developed across L1b.

• The feedback voltage L1bis in phase with the input voltage across L1aand hence results in oscillations.

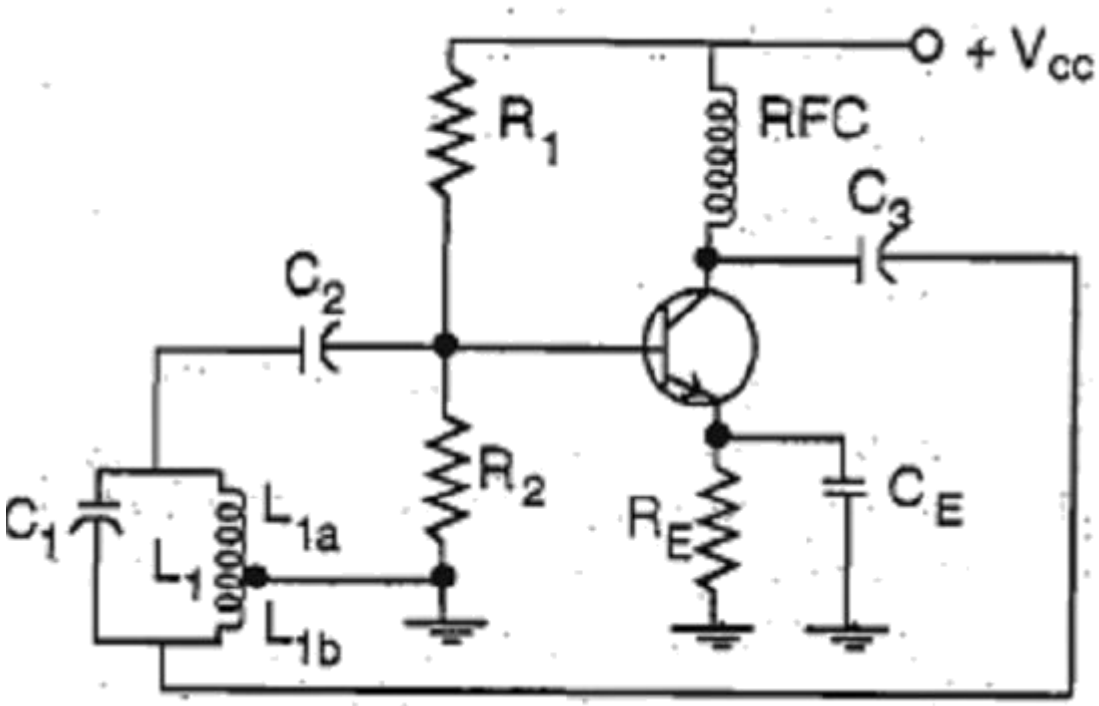


The F.B voltage is in phase with the input voltage as180°phase shift occurs between

signal at base and collector, and another 180°is being provided by the fact that the two ends of coil L1 are of opposite polarity.

• The capacitor C3 blocks the dc components of collector circuit but couples ac signal.

• The dc components flows to Vcc supply through r-f choke which also prevents ac components from following this path as RFC acts as a dc short and ac open.



The value of L,C determine the frequency of oscillation:

$$f = \frac{1}{2\pi\sqrt{LC}}$$

Remark

Radio frequency inductor

• (RF), inductors have radio frequencies , particularly high frequencies At higher resistance and other losses. In addition to causing power loss, in of the circuit, broadening Q factor this can reduce the resonant circuits .RF inductors, are specialized construction techniques bandwidth the which used to minimize these losses.

Hartley Oscillator:-

Description:

• The Hartley oscillator is designed for generation of sinusoidal oscillations in the R.F range (20 KHz -30 MHz).

• It is very popular and used in radio receivers as a local oscillator.

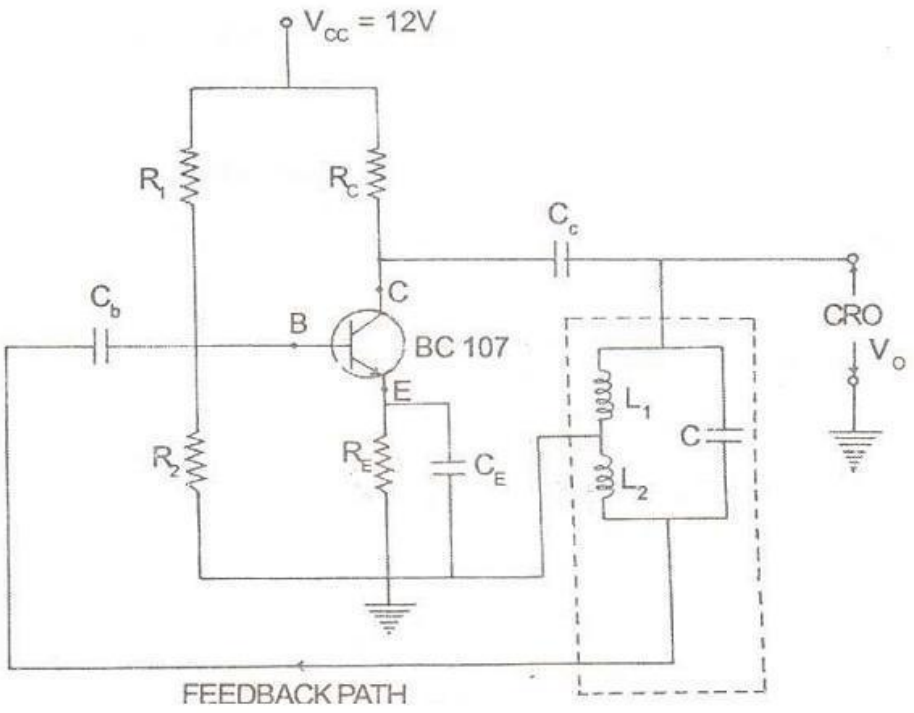
H.O

• The circuit diagram consists of an CE amplifier configuration.

• R1and R2form a voltage divider.

• The coupling capacitor Cc blocks dc and provides an ac path from the collector to the tank circuit.

• The feedback network (L1, L2and C) determines the frequency oscillation of the oscillator.

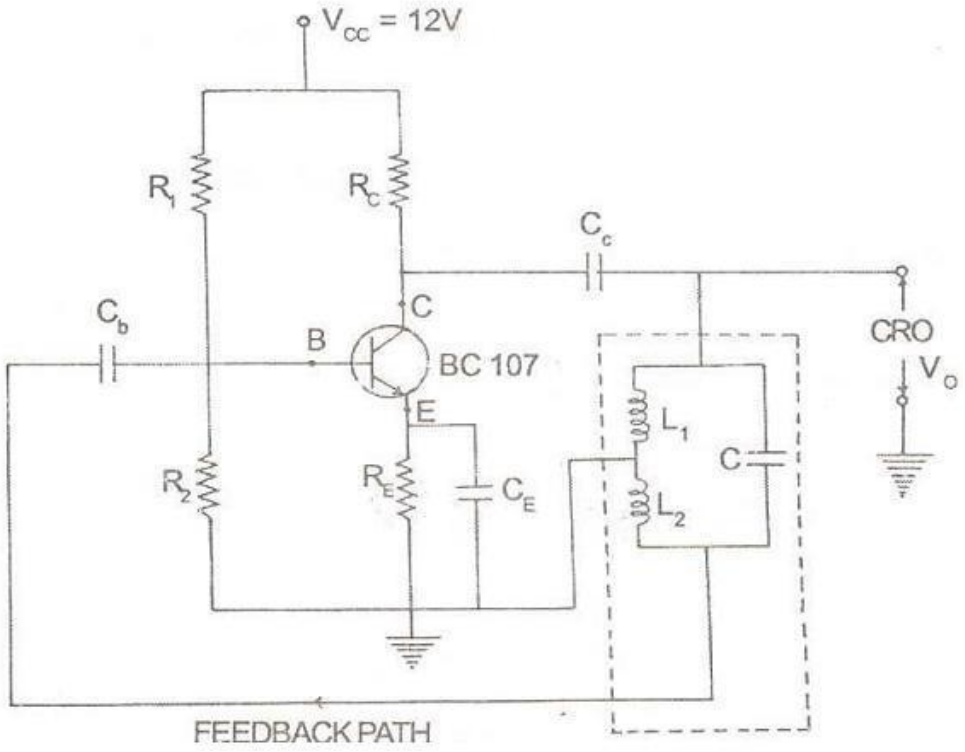


H.O

• When the collector supply voltage Vcc is switched on, due to some transient disturbances in the circuit the collector current starts rising and charges the capacitor C.

• It discharges through coils L1and L2, setting up oscillations in the tank circuit.

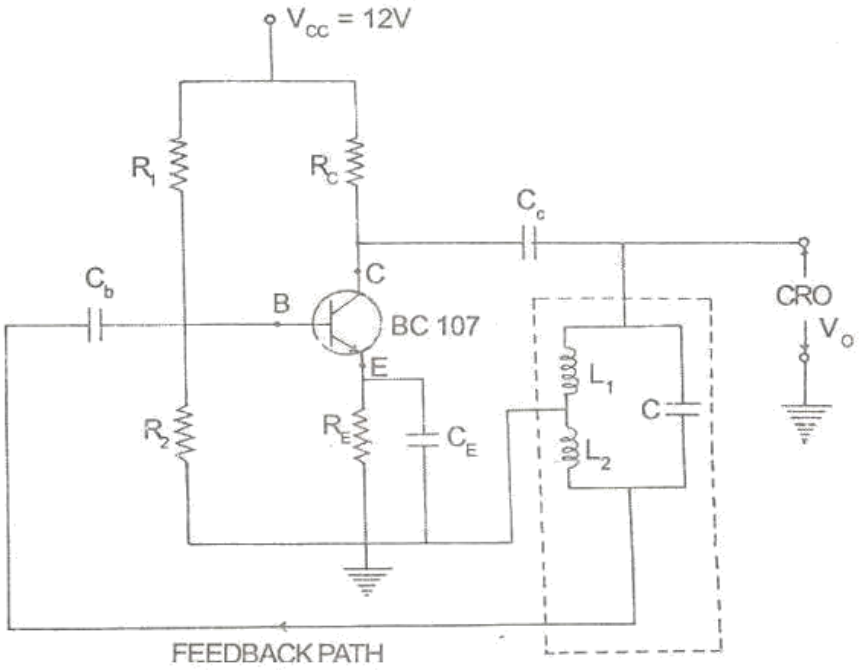
• The oscillatory current in the tank circuit produces an a.c voltage which is applied to the base emitter junction of the transistor and appears in the amplified form in the collector circuit.



• The phase difference between the voltages across L1and that across L2is always 180°because the centre of the two is grounded.

• A further phase of 180°is introduced between the input and output the voltages by transistor itself.

• Thus the total phase shiftbecomes 360°(or zero), thereby making the feedback positive or regenerative which is essential for oscillations. So continuous oscillations are obtained.



The Crystal Oscillation

• A crystal oscillator is a tuned circuit using a crystal as a resonant circuit. Oscillator provides great frequency stability.

• They use crystal slices, usually made of quartz. The crystal materials exhibits the piezoelectric effect. When the voltage is applied across a piezoelectric (usually quartz),

• The crystal oscillates in a stable and accurate manner. The frequency of oscillation is determined by the crystal dimensions.

• Commercial quartz crystals are ready available with frequencies from a few kilohertz to a few hundred megahertz.

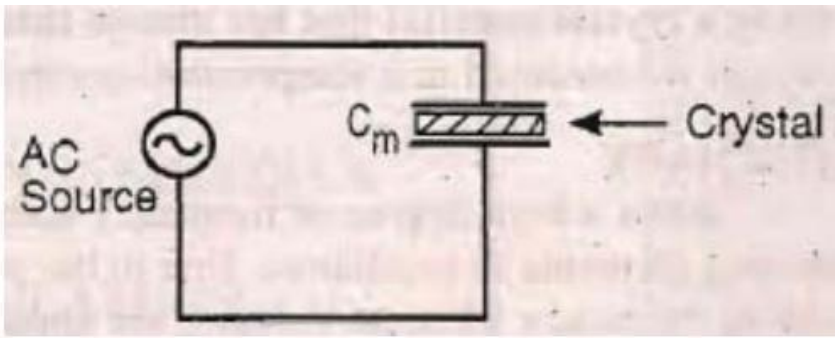
• If mechanical pressure is put on such a crystal, electrical charges appear across

its faces, and an ac voltage can be generated.

• If a crystal is excited by an ac voltage the crystal generates a significant ac voltage. For use in electronic circuit , the crystal is cut and mounted between two metal plates.

Consider that an acsource is connected across it . when the mounted crystal is not vibrating ,it is equivalent to a capacitance Cm because it has two metal plates separated by a dielectric .

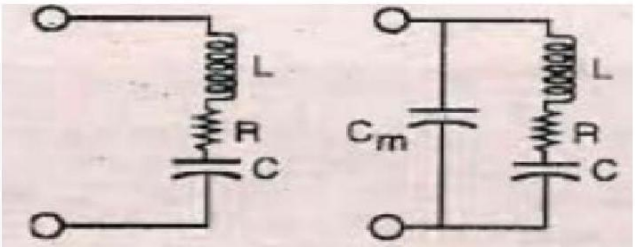
• When ac voltage is applied to the crystal ,it starts vibrating .

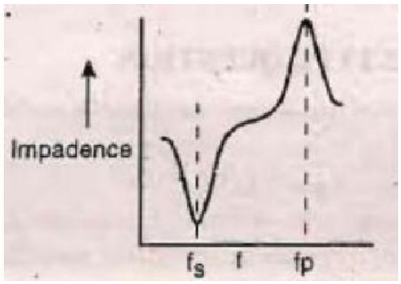


the natural resonant frequency depends on the type of material, how it is cut and its physical dimensions.

• The natural frequency of a crystal is inversely proportional to its thickness.

• This property of crystals make them highly useful in the oscillator circuits.





The crystal has two resonant frequencies. The crystal behaves as a parallel resonant circuit at a frequency at which the series LCR branch has an inductive reactance which equal to the capacitive reactance of Cm.

• This parallel combinationoffers maximum impedance . The series resonant frequency fsof crystal is the resonant frequency of LCR branch. At this frequency, the impedance of LCR branch is minimum.

Colpitts Crystal Oscillator

- This figure shows a Colpitts crystal oscillator .
- The input signal to the base of the transistor is inverted at the transistors output.
- The output signal at the collector is then taken through a 180^{o} phase shifting network which includes the crystal operating in a series resonant mode.