VEER SURENDRA SAI UNIVERSITY OF TECHNOLOGY:BURLA
(Formerly University College of Engg.,Burla-Established by Govt. of Odisha in 1956 &
Upgraded in 2009 to A State Govt. University covered under Section 2(f) & 12(B) of UGC Act.)
P.O: Engineering College, Burla (Siddhi Vihar),Dist: Sambalpur
Odisha-768018, India, www.vssut.ac.in

No. VSSUT/Estt/ 57 Dated 09/01/2023

WALK-IN INTERVIEW FOR GUEST FACULTY

Candidates possessing B.E/B.Tech and M.E/M.Tech or Integrated M.Tech in relevant branch with First Class degree or equivalent, i.e. 60% or 6.5 CGPA in **Electrical Engineering** with consistently good academic records in relevant field are invited to attend an interview on **16.01.2023** at **10:00 A.M** in the Electrical Engineering Department of VSSUT, Burla, for engagement as Guest Faculty for the Even Semester 2022-23 with a consolidated remuneration as follows:

i) Rs.50,000/- and Rs. 55,000/- for candidates with M.Tech and Ph.D Degree in Engineering respectively.

Interested candidates are required to come physically with their resumes, two recent passport size colour photographs, one set of xerox copies of all certificates, mark sheets and other relevant documents in support of their qualifications and experience, if any, along with the originals for verification and an amount of Rs.1000/- (Rs.500/- in case of SC/ST candidates) to be deposited at cash counter of VSSUT, Burla. No TA/DA is admissible for attending the interview.

The authority reserves the right to reject any or all the applications or cancel the entire selection process without assigning any reason thereof.

09/01/2023
REGISTRAR (I/C)

Memo No. VSSUT/Estt./ 58 Dated 09/01/2023

Copy to:

1. The Director, I&PR Department, Government of Odisha, Bhubaneswar for information with a request to publish the above advertisement in all Odisha daily edition of the SAMAJ on or before 11.01.2023.
2. University Notice Board.
3. The Dean, Faculty & Planning with a request to display the advertisement in University website immediately.
4. The Dean, Academic Affairs/COF for information & necessary action.
5. PA to V.C. for kind information of the Vice Chancellor.
6. PA to Registrar for kind information.

09/01/2023
REGISTRAR (I/C)

Memo No. VSSUT/Estt./ 59 Dated. 09/01/2023

Copy to HOD Electrical Engineering for information with a request to conduct the interview in their Department on the schedule date and time with the help of members of the Selection Committee recommended by the HOD and approved by the Vice Chancellor. He is further requested to submit the merit list of selected candidates along with the proceedings and evaluation sheets to the undersigned on or before 17.01.2023 for taking necessary action.

09/01/2023
REGISTRAR (I/C)