Course Structure & Syllabus
of
M. Tech. Programme
in
Electronics & Telecommunication Engineering
with Specialization
VLSI SIGNAL PROCESSING
Academic Year – 2019-20

VEER SURENDRA SAI UNIVERSITY OF TECHNOLOGY, ODISHA
Burla, Sambalpur-68018, Odisha
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DEPARTMENT VISION:

Developing new ideas in the field of communication to enable students to learn new technologies, assimilate appropriate skills and deliver meaningful services to the global society and improve the quality of life by training them with strength of character, leadership and self-attainment.

DEPARTMENT MISSION:

- Imparting futuristic technical education to the students.
- Promoting active role of Industry in student curriculum, projects, R&D and placements. Organizing collaborative academic and non-academic programmes with institutions of national and international repute for all round development of students.
- Organizing National and International seminars and symposium for exchange of innovation, technology and information.
- Expanding curricula to cater to demands of higher studies in internationally acclaimed institutes. Preparing students for promoting self-employment.
- Develop the department as a center of excellence in the field of VLSI and communication technology by promoting research, consultancy and innovation.

VEER SURENDRA SAI UNIVERSITY OF TECHNOLOGY, ODISHA, BURLA
Department of Electronics & Telecommunication Engineering

Course Structure & Curriculum of M. Tech Programme in
VLSI SIGNAL PROCESSING

Sl. No.	Core/ Elective	Subject Code	Subject Name	L	T	P	Cr
			SEMESTER-I				
1	Core-1		Analog CMOS VLSI Design	3	0	0	3
2	Core-2		Advanced Signal Processing	3	0	0	3
3	PE-1			3	0	0	3
4	PE-2			3	0	0	3
5	Common		Research Methodology & IPR	2	0	0	3
6	Lab-1		VLSI Design Laboratory-I	0	0	3	2
7	Lab-2		VLSI Technology Laboratory	0	0	3	2
8	Audit-1		English for Research Paper Writing				
			Total Credits				**19**
			SEMESTER-II				
1	Core-3		VLSI Signal Processing	3	0	0	3
2	Core-4		Digital Signal Processor Architecture	3	0	0	3
3	PE-3			3	0	0	3
4	PE-4			3	0	0	3
5	Common		Term Paper	0	0	4	2
6	Lab-3		VLSI Design Laboratory-II	0	0	3	2
7	Lab-4		VLSI Signal Processing Laboratory	0	0	3	2
8	Audit-2		Pedagogy Studies				
			Total Credits				**18**
			SEMESTER-III				
1	PE-5			3	0	0	3
2	OE-1			3	0	0	3
3	Minor Project		Project Progress Report	0	0	20	10
			Total Credits				**16**
			SEMESTER-IV				
1	Major Project		Project & Thesis	0	0	32	16
			Total Credits				**16**
			Grand Total Credits				**69**

Sl. No.	Category	Subject Name
1	PE-1	Digital CMOS VLSI Design
2		Electronic Design Automation
3		VLSI Algorithm
1	PE-II	VLSI Technology
2		Semiconductor Device Modelling
3		JTFA & MRA
1	PE-III	High Level VLSI Design
2		RTL Simulation & Synthesis
3		CAD of Digital Systems
1	PE-IV	VLSI Design Verification & Testing
2		Low Power VLSI Design
3		Design with ASIC
1	PE-V	RF IC
2		FPGA Based DSP Design
3		Physical Design Automation
1	OE	Signal Processing
2		Basics of VLSI Engineering
3		Audio & Video Systems

ANALOG CMOS VLSI DESIGN (Core-1)

COURSE OBJECTIVE

1. Learning the concepts of designing analog integrated circuits in the context of CMOS technology which enable the students to understand the operation of an analog CMOS circuit and to know how to change its performance.
2. Knowing the key subjects of MOSFET large-signal and small signal model to predict the performance of CMOS circuit.
3. Designing of two stage op-amp with methods of compensation and to know how uncompensated two stage op-amp acts as open loop comparator.

MODULE	CONTENTS	HOURS
MODULE 1	***MOS Device and Modeling***: The MOS Transistor, Passive Components- Capacitors and Resistors, Integrated Circuit Layout, CMOS Device Modeling- Simple MOS Large Signal Model, Other MOS Large Signal Model Parameters, Small Signal Model of the MOS Transistor, Computer Simulator Models, Subthreshold MOS Model.	06
MODULE 2	***Analog CMOS Sub Circuits***: MOS Switch, MOS Diode/Active Resistor, MOS Current Sinks and Sources, Current Mirrors- Current Mirror with Beta Helper, Cascode Current Mirror and Wilson Current Mirror, Voltage and Current References, Bandgap Reference.	08
MODULE 3	***CMOS Amplifiers***: Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers.	10
MODULE 4	***CMOS Operational Amplifiers***: Design of Op-Amps, Compensation of OP-Amps, Design of a Two-Stage OP-Amp, Power Supply Rejection Ratio of Two Stage Op-Amp.	08
MODULE 5	***Comparators:*** Characterization of a Comparator, Two Stage Open Loop Comparators, Discrete Time Comparators. Other Open Loop Comparators, Improving the Performance of Open Loop Comparators.	08
TEXT BOOKS	1. Philip.E. Allen and Douglas.R. Holberg, "*CMOS Analog Circuit Design*", Oxford University Press, Indian3rd Edition, 2012. 2. Paul.R. Gray, Paul.J. Hurst, S.H. Lewis and R.G.Meyer, "*Analysis and Design of Analog Integrated Circuits"*, Wiley India, Fifth Edition, 2010.	
REFERENCE BOOKS	1. 1.R.J. Baker, H. W. Li, D. E. Boyce, "*CMOS Circuit Design, Layout, and Simulation"*, PHI, 2002 2. D.A. Johns and K. Martin, "*Analog Integrated Circuit Design*"; Wiley Student Edition, 2013 3. B. Razavi, "*Design of Analog CMOS Integrated Circuits*", Tata McGraw-Hill, 2002.	

COURSE OUTCOME|

After completion of this course, students should be able to

1. Know the key subjects of MOSFET large-signal and small signal model to predict the performance of CMOS circuit.
2. To visualize how sub circuits and amplifiers are used to design more complex analog circuits, such as op-amp.
3. Learn the design procedures of different CMOS amplifier circuits.
4. Design two stage op-amp with methods of compensation and to know how uncompensated two stage op-amp acts as open loop comparator.
5. Characterize different comparator circuits and improve their performances.

ADVANCED SIGNAL PROCESSING (Core-2)

COURSE OBJECTIVE

This subject aims to provide the students to

1. Analyze the process of Sampling, aliasing and the relationship between discrete and continuous signals. Review of Fourier transforms, the Z-transform, FIR and IIR filters, and oscillators
2. Implement the Filter design techniques, structures and numerical round-off effects. Understand the Auto-correlation, cross-correlation, power spectrum estimation techniques, forward and backward Linear prediction
3. Analyze Wiener filters, LMS adaptive filters, and applications, Multi-rate signal processing and sub-band transforms. Analyze the Time-frequency analysis, the short time Fourier transform, and wavelet transforms.

MODULE	CONTENTS	HOURS
MODULE 1	***Multi-Rate Digital Signal Processing***: Introduction, Decimation by A Factor D, Interpolation by A Factor I, Sampling Rate Conversion by Rational Factor I/D, Filter Design and Implementation for Sampling-Rate, Multistage Implementation of Sampling Rate Conversion, Sampling Rate Conversion of Band-Pass Signal, Application of Multi Rate Signal Processing: Design of Phase Shifters, Implementation pf Narrowband Low Pass Filters. Implementation of Digital Filter Banks	8
MODULE 2	***Linear Prediction and Optimum Linear Filters***: Innovations Representation of a Stationary Random Process, Forward and Backward Linear Prediction, Solution of The Normal Equations, Properties of The Linear Prediction Error Filters, AR Lattice and ARMA Lattice-Ladder Filters, Wiener Filter For Filtering and Prediction: FIR Wiener Filter, Orthogonality, Principle in Linear Mean-Square Estimation.	8
MODULE 3	***Power Spectrum Estimation***: Estimation of Spectra from Finite-Duration Observation of Signals, Non-Parametric Method for Power Spectrum Estimation: Bartlett Method, Blackman And Turkey Method, Parametric Method for Power Estimation: Yuke-Walker Method, Burg Method, MA Model and ARMA Model. Filter Bank and - Filters and Its Applications	8
MODULE 4	Adaptive Signal Processing Least Mean Square Algorithm, Recursive Least Square Algorithm, Variants of LMS Algorithm: SK-LMS, N-LMS, FX-LMS. Adaptive FIR & IIR Filters, Application of Adaptive Signal Processing: System Identification, Channel Equalization, Adaptive Noise Cancellation, Adaptive Line Enhancer.	10
MODULE 5	HOS- Higher Order Statistics: Definitions and Properties, Moments, Cumulants, Blind Parameters and Order Estimation of MA & ARMA Systems. Application of Higher Order Statistics: Applications to Signal Processing and Image Processing.	6

TEXT BOOKS	1. J.G. Proakis and D.G. Manolakis, "Digital Signal Processing", 3rd Edition, PHI.
REFERENCE BOOKS	1. Oppenheim and Schafer, "Digital Signal Processing", PHI 2. B. Widrow and Stern, "Adaptive Signal Processing", PHI,1985

COURSE OUTCOME

After completion of this course, students should be able to

1. Have a more thorough understanding of the relationship between time and frequency domain interpretations.
2. Implementations of signal processing algorithms.
3. Be familiar with some of the most important advanced signal processing techniques, including multi-rate processing and time-frequency analysis techniques
4. Understanding power spectrum estimation techniques.
5. Understand and be able to implement adaptive signal processing algorithms based on second order statistics.

DIGITAL CMOS VLSI DESIGN (PE-1)

COURSE OBJECTIVE

1. Study the characteristics of MOS as an Inverter.
2. Study the behavior of MOS in combinational circuits.
3. Study the behavior of MOS in sequential circuits.

MODULE	CONTENTS	HOURS
MODULE 1	***Introduction to MOSFETs***: MOS Inverter, Static and Switching Characteristics, Voltage Transfer characteristics, Noise Margin, Regenerative Property, Power and Energy Consumption, Stick/Layout Diagrams; Issues of Scaling.	08
MODULE 2	***Combinational MOS Logic Circuits***: Pass Transistors, Transmission Gates, Primitive Logic Gates; Complex Logic Circuits.	08
MODULE 3	***Sequential MOS Logic Circuits***: Latches and Flip-flops, Dynamic Logic Circuits; Clocking Issues, Rules for Clocking, Performance Analysis, Logical effort.	08
MODULE 4	***CMOS Subsystem Design***; Data Path and Array Subsystems: Addition, Subtraction, Comparators, Counters, Coding, Multiplication and Division.	08
MODULE 5	***Memory Design:*** SRAM, DRAM, ROM, Serial Access Memory, Content Addressable Memory, Field Programmable Gate Array.	08
TEXT BOOKS	1. Rabey J.M, A. Chandrakasan, and B.Nicolic, "*Digital Integrated Circuits: A design Perspective*", Second Edition, Pearson/PH, 2003 (Cheap Edition). 2. N.H.E. Weste and D.M. Harris, "*MOS VLSI design: A Circuits and Systems Perspective*", 4th Edition, Pearson Education India, 2011	
REFERENCE BOOKS	1. Kang, Sung-Mo, and Yusuf Leblebici. "*CMOS Digital Integrated Circuits*", Tata McGraw-Hill Education, 2003.	

COURSE OUTCOME

After completion of course student should be able to

1. Extract the MOS switching parameters.
2. Carryout efficient design of combinational circuits.
3. Design the sequential circuits.
4. Realize logic circuits with different design styles.
5. Demonstrate an understanding of working principle of operation of different types of memory.

ELECTRONIC DESIGN AUTOMATION (PE-1)

COURSE OBJECTIVE

1. Study of Electronic design automation at various levels of IC design.
2. Study of automation in electronic system-level design and high-level synthesis.
3. Study of automation in fault simulation and test generation.

MODULE	CONTENTS	HOURS
MODULE 1	***Introduction:*** Overview of Electronic Design Automation, Logic Design Automation, Test Automation, Physical Design Automation.	08
ODULE 2	***Design for Testability***: Introduction, Testability Analysis, Scan Design, Logic Built-In Self-Test, Test Compression.	08
MODULE 3	***Fundamentals of Algorithms***: Introduction, Computational Complexity, Asymptotic Notations, Complexity Classes, Graph Algorithms, Heuristic Algorithms, Mathematical Programming,	08
MODULE 4	***Electronic System-Level Design and High-Level Synthesis***: Introduction, Fundamentals of High-Level Synthesis, High-Level Synthesis Algorithm Overview, Scheduling, Register Binding, Functional Unit Binding. ***Logic and Circuit Simulation:*** Introduction, Logic Simulation Models, Timing Models, Logic Simulation Techniques, Hardware-Accelerated Logic Simulation, Circuit Simulation Models, Numerical Methods for Transient Analysis.	08
MODULE 5	***Functional Verification***: Introduction. Verification Hierarchy, Measuring Verification Quality. Simulation-Based Approach, Formal Approaches. ***Fault Simulation and Test Generation***: Introduction, Fault Collapsing, Fault Simulation, Test Generation.	08
TEXT BOOKS	1. Laung-Terng Wang, Yao-Wen Chang.`Kwang-Ting (Tim) Cheng, "*Electronic Design Automation: Synthesis, Verification, and Test*", Morgan Kaufmann Publishers is an imprint of Elsevier. 2. Mark Birnbaum, "*Essential Electronic Design Automation (EDA)*", Prentice Hall Modern Semiconductor Design Series.	
REFERENCE BOOKS	1. Dirk Jansen, "*The Electronic Design Automation Handbook*", Kluwer Academic Publishers Norwell, MA, USA ©2003, ISBN:14020750223.	

COURSE OUTCOME

After completion of this course, students should be able to

1. Grasp the overview of electronic design automation at various stages of IC fabrication.
2. Learn the automation techniques of IC design for testability.
3. Know different algorithms for IC design.
4. How automation is being carried out in electronic system-level design and high-level synthesis.
5. Learn to implement automation in functional verification, fault simulation and test generation.

VLSI ALGORITHMS (PE-1)

COURSE OBJECTIVE:

1. Study of VLSI automation algorithms.
2. Study of Global routing.
3. Study of cell routing & via minimization

MODULE	CONTENTS	HOURS
MODULE 1	***VLSI Automation Algorithms***: General Graph Theory and Basic VLSI Algorithms. ***Partitioning***: Problem Formulation, Classification of Partitioning Algorithms, Group Migration Algorithms, Simulated Annealing & Evolution, Other Partitioning Algorithms.	
MODULE 2	***Placement, Floor Planning & Pin Assignment***: Problem Formulation, Simulation Base Placement Algorithms, Other Placement Algorithms, Constraint-Based Floor Planning, Floor Planning Algorithms for Mixed Block & Cell Design. General & Channel Pin Assignment.	
MODULE 3	***Global Routing***: Problem Formulation, Classification of Global Routing Algorithms, Maze Routing Algorithm, Line Probe Algorithm, Steiner Tree Based Algorithms, ILP Based Approaches. ***Detailed Routing***: Problem Formulation, Classification of Routing Algorithms, Single Layer Routing Algorithms, Two-Layer Channel Routing Algorithms, Three-Layer Channel Routing Algorithms, And Switchbox Routing Algorithms.	
MODULE 4	***Over the Cell Routing & Via Minimization***: Two Layers Over the Cell Routers Constrained & Unconstrained Via Minimization.	
MODULE 5	***Compaction***: Problem Formulation, One-Dimensional Compaction, Two Dimensions-Based Compaction, Hierarchical Compaction.	
TEXT BOOKS	1. Naveed Shervani, "*Algorithms for VLSI Physical Design Automation*", Academic Publisher, Edition, 2005. Kluwer 2. Thorsten Theobald, "*Algorithm and Data Structures for VLSI Design*", KAP, 2002.	
REFERENCE BOOKS	1. Rolf Drechsheler "*Evolutionary Algorithm For VLSI*", Second Edition, 2002. 2. Trimburger," *Introduction to CAD For VLSI*", Kluwer Academic Publisher, 2002.	

COURSE OUTCOME

After completion of this course, students should be able to

1. Formulate floor partitioning.
2. Make Placement, Floor Planning & Pin Assignment.
3. Implement multilayer routing.
4. Carryout over the Cell Routing & Via Minimization.
5. Do perfect compaction.

VLSI TECHNOLOGY (PE-2)

COURSE OBJECTIVE:

1. To understand the Fabrication of ICs and purification of Silicon in different technologies
2. To impart in-depth knowledge about Etching and deposition of different layers.
3. To understand the different packaging techniques of VLSI devices.

MODULE	CONTENTS	HOURS
MODULE 1	***Crystal Growth, Wafer Preparation, Epitaxy and Oxidation*:** Metallurgical Grade Silicon, Electronic Grade Silicon, Czochralski Crystal Growing, Silicon Shaping, Etching, Polishing, Chemical Cleaning, Gettering Treatment, Vapor Phase Epitaxy, Epitaxial Evaluation, Growth Mechanism.	10
MODULE 2	***Oxidation***: Oxidation Growth Mechanism and Kinetic Oxidation, Oxidation Techniques and Systems, Oxide Properties, Oxide Induced Defects, Characterization of Oxide Films, Use of Thermal Oxide and CVD Oxide, Growth and Properties of Dry and Wet Oxide, Dopant Distribution, Oxide Quality. ***Diffusion:*** Introduction, Diffusion Equipment and Process, Diffusion Models, Modification of Flick's Law, Oxidation Effects on Diffusion.	8
MODULE 3	***Ion Implantation*** – Range Theory, Equipment's, Ion Implantation Parameter Affecting the Dose and Uniformity, Implant Damage and Annealing, ***Etching***: Wet Chemical Etching, Dry Etching. ***Lithography***: Introduction, Photolithographic Process, Photo Resist, Non-Photo Resist, Light Source and Optical Exposure Systems, Pattern Transferring Techniques and Mask Aligner, Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography.	8
MODULE 4	***Dielectric and Polysilicon Film Deposition:*** Introduction, Deposition Process, Chemical Vapor Deposition, Physical Vapor Deposition, Polysilicon, Silicon Dioxide, Silicon Nitride, Plasma Assisted Deposition. ***Metallization*** - Different Types of Metallization, Uses & Desired Properties. ***IC Manufacturing***: Electrical Testing, Packaging, Yield.	8
MODULE 5	BJT Fabrication and Realization, Overview of MOS Transistor, ***MOS Transistor Process Flow***: MOS Transistor Fabrication, Device Isolation, CMOS Fabrication, Latch - Up In CMOS, BICMOS Technology.	6

TEXT BOOKS	1. Gary S. May, Simon M. Sze, "*Fundamentals of Semiconductor Fabrication*", John Wiley Inc.,2004 2. Stephen Cambell, "*The Science and Engineering of Microelectronic Fabrication*", Oxford University Press, 2001.
REFERENCE BOOKS	1. Gauranga Bose, "*IC Fabrication Technology*", McGraw hill Education 2. J. D. Plummer, M. D. Deal and P. B. Griffin, "*Silicon VLSI Technology Fundamentals*", Practice and Models, Prentice Hall, 2000. 3. Nandita Das Gupta, "*VLSI Technology*", NPTEL Courseware.

SEMICONDUCTOR DEVICE MODELLING (PE-2)

COURSE OBJECTIVE

1. To understand the device parameters and characteristics and their implementation in SPICE.
2. Modelling of diode, BJT and MOS transistor.
3. Understand the effect of noise and distortion on device modelling.

MODULE	CONTENTS	HOURS
MODULE 1	***PN Junction Diode and Schottky Diode***: DC Current Voltage Circuits, Static Model, Large Signal Model, Small Signal Model, Schottky Diode and Its Implementation in SPICE 2, Temperature and Area Effect on The Diode Model Parameters, SPICE3, HSPICE & PSPICE Models.	08
MODULE 2	***BJT:*** Transistor Conversion and Symbols, Ebers-Moll Static, Large Signal and Small Signal Models, Gummel-Poon Static, Large Signal Models, Temperature and Area Effect on The BJT Parameters, Power BJT Models, SPICE3, HSPICE & PSPICE Models.	08
MODULE 3	***JFET:*** Static Model, Large Signal Model, Small Signal Model and Its Implementation in SPICE 2, Temperature and Area Effect on The JFET Model Parameters, SPICE3, HSPICE & PSPICE Models	08
MODULE 4	***Metal Oxide Semiconductor Transistor (MOST):*** Structure and Operating Regions of the MOST, Level-1 And Level-2 Static Models, Level-1 And Level-2 Large-Signal Models, Comment on The Three Models, The Effect of Series Resistance, Small-Signal Models, The Effect of Temperature on The MOST Model Parameters, BSIM1 & BSIM2 Models, SPICE3, HSPICE & PSPICE Models	10
MODULE 5	***Noise and Distortion***: Noise, Distortion In MOSEFT, ISFET, THYRISTOR.	06
TEXT BOOKS	1. G. Massobrio and P.Antognetti, "*Semiconductor Device Modeling by SPICE"*, Second Edition, McGraw Hill, 1993.	
REFERENCE BOOKS	1. N. Dasgupta and A. Dasgupta, "*Semiconductor Device Modeling"*, PHI Publication	

COURSE OUTCOME

After completion of this course, students should be able to

1. Model a diode.
2. Model a BJT.

3. Model a JFET
4. Model a MOSFET.
5. Model noise and distortion

JTFA & MRA (PE-2)

COURSE OBJECTIVE:

1. Introduction to Transforms in signal processing
2. To understand Time -Frequency Analysis & Multiresolution Analysis
3. Study of Wavelets and its Applications

MODULE	CONTENT	HOURS
MODULE 1	***Introduction***: Review of Fourier Transform, Parseval Theorem and Need for Joint Time-Frequency Analysis (JTFA), Concept of Non-Stationary Signals, Short-Time Fourier Transforms (STFT), Uncertainty Principle, And Localization/Isolation in Time and Frequency, Hilbert Spaces, Banach Spaces, And Fundamentals of Hilbert Transform.	8
MODULE 2	***Bases for Time-Frequency Analysis***: Wavelet Bases and Filter Banks, Tilings Of Wavelet Packet and Local Cosine Bases, Wavelet Transform, Real Wavelets, Analytic Wavelets, Discrete Wavelets, Instantaneous Frequency, Quadratic Time-Frequency Energy, Wavelet Frames, Dyadic Wavelet Transform, Construction of Haar And Roof Scaling Function Using Dilation Equation and Graphical Method.	8
MODULE 3	***Multiresolution Analysis***: Haar Multiresolution Analysis (MRA), MRA Axioms, Spanning Linear Subspaces, Nested Subspaces. Orthogonal Wavelets Bases, Scaling Functions, Conjugate Mirror Filters, Haar 2-Band Filter Banks. Study of Up Samplers and Down Samplers. Conditions for Alias Cancellation and Perfect Reconstruction. Discrete Wavelet Transform and Relationship with Filter Banks. Frequency Analysis of Haar 2-Band Filter Banks, Scaling and Wavelet Dilation Equations in Time and Frequency Domains, Case Study of Decomposition and Reconstruction of Given Signal Using Orthogonal Framework of Haar 2 Band Filter Bank.	8
MODULE 4	***Wavelets:*** Daubechies Wavelet Bases, Daubechies Compactly Supported Family of Wavelets, Daubechies Filter Coefficient Calculations, Case Study of Daub-4 Filter Design, Connection Between Haar And Daub-4, Concept of Regularity, Vanishing Moments. Other Classes of Wavelets Like Shannon, Meyer, And Battle-Lamarie.	6
MODULE 5	***Bi-Orthogonal Wavelets and Applications***: Construction and Design. Case Studies of Biorthogonal 5/3 Tap Design and Its Use in JPEG 2000. Wavelet Packet Trees, Time-Frequency Localization, Compactly Supported Wavelet Packets, Case Study of Walsh Wavelet Packet Bases Generated Using Haar Conjugate Mirror Filters till Depth	10

	Level 3. Lifting Schemes for Generating Orthogonal Bases of Second-Generation Wavelets. ***JTFA Applications***: Riesz Bases, Scalograms, ***Time-Frequency Distributions***: Fundamental Ideas, ***Applications:*** Speech, Audio, Image and Video Compression; Signal Denoising, Feature Extraction, Inverse Problem.	
TEXT BOOK	1. S. Mallat, "*A Wavelet Tour of Signal Processing*," 2nd Edition, Academic Press, 1999. 2. L. Cohen, "*Time-frequency analysis*," 1st Edition, Prentice Hall, 1995. 3. G.Strang and T. Q. Nguyen, "*Wavelets and Filter Banks*," 2nd Edition, Wellesley Cambridge Press, 1998.	
REFERENCE BOOK	1. Daubechies, "Ten Lectures on Wavelets," SIAM, 1992. 2. P. P. Vaidyanathan, "*Multirate Systems and Filter Banks*," Prentice Hall, 1993. 3. M. Vetterli and J. Kovacevic, "*Wavelets and Sub band Coding*", Prentice Hall, 1995	
COURSE OUTCOME: After completion of course, student should be able to 1. Get a survey on evolution of JTFA from the classical transforms 2. Realize the role of wavelets as bases of time-frequency analysis 3. Have an in-depth theoretical & mathematical investigation of wavelets 4. Explore the applications of wavelets and JTFA 5. Understand application of wavelets in compression.		

VLSI DESIGN LABORATORY-I (Lab-1)

SESSIONAL OBJECTIVE

1. Design of sub circuits to complex circuits
2. Simulation of analog circuits by CAD tools.
3. Use of industry standard software.

No.	CONTENTS
1	Design and Simulation of Current Mirror Circuits
2	Design and Simulation of Reference Circuits
3	Design and Simulation of Amplifiers
4	Design and Simulation of CMOS OP-Amp
5	Design and Simulation of Comparators

VLSI TECHNOLOGY LABORATORY (Lab-2)

SESSIONAL OBJECTIVE

1. Study of different fabrication processes.
2. Study of materials used for fabrication.
3. Use of industry standard software.

No.	CONTENTS
1	Study of crystal Growth and Wafer Preparation
2	Study of Epitaxial Growth
3	Study of Oxidation

4	Study of Lithography
5	Study of Etching
6	Study of Deposition
7	Study of Diffusion
8	Study of Ion Implantation
9	Study of Metallization
10	Study of Packaging

VLSI SIGNAL PROCESSING (Core-3)

COURSE OBJECTIVE

1. To review VLSI design methods. To explore VLSI architecture.
2. To implement DSP algorithms onto digital hardware.
3. Applications of parallel processing and pipelining.

MODULE	CONTENTS	HOURS
MODULE 1	***Pipelining and Parallel Processing***: Introduction, Pipelining of FIR Digital Filters, Parallel Processing. ***Pipelining and Parallel Processing for Low Power. Retiming***: Introduction, Definition and Properties, Solving System of Inequalities, Retiming Techniques.	06
MODULE 2	***Unfolding***: Introduction an Algorithms for Unfolding, Properties of Unfolding, Critical Path, Unfolding and Retiming Application of Unfolding.	06
MODULE 3	***Folding***: Introduction to Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding in Multirate Systems.	08
MODULE 4	***Systolic Architecture Design***: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations Containing Delays.	10
MODULE 5	***Fast Convolution***: Introduction, Cook, Toom Algorithm, Winogard Algorithm, Iterated Convolution, Cyclic Convolution, Design of Fast Convolution Algorithm by Inspection.	10
TEXT BOOKS	1. Keshab K. Parhi. "*VLSI Digital Signal Processing Systems"*, Wiley-Inter Sciences, 1999	
REFERENCE BOOKS	1. Mohammed Ismail, Terri, Fiez, "*Analog VLSI Signal and Information Processing",* McGraw Hill, 1994. 2. Kung. S.Y., H.J. While house T.Kailath, "*VLSI and Modern signal processing",* Prentice Hall, 1985. 3. Jose E. France, Yannis Tsividls, "*Design of Analog Digital VLSI Circuits for Telecommunications and Signal Processing",* Prentice Hall, 1994.	

COURSE OUTCOME

After completion of course student should be able to

1. Understand VLSI design methodology for signal processing systems. Be familiar with VLSI algorithms and architectures for DSP.
2. Be able to implement basic architectures for DSP using CAD tools.
3. Design and analysis of FIR digital filters using pipelined architecture.
4. Design and analysis of FIR digital filters using parallel processing.
5. Implementing Cook, Toom Algorithm, Winogard Algorithms.

DIGITAL SIGNAL PROCESSOR ARCHITECTURES (Core-4)

COURSE OBJECTIVE

1. To shift gradually from the design of DSP systems and algorithms to efficient implementation of the systems and algorithms.
2. To give an exposure to the concepts of real-time DSP and bridge the gap between theoretical signal processing and real-time implementations.
3. To know how the DSP processor is used in an embedded system with a minimum amount of external hardware to support its operation and interface it to the outside world

MODULE	CONTENTS	HOURS
MODULE 1	***Introduction***: A Digital Signal-Processing System, Analysis and Design Tool for DSP Systems, ***Computational Accuracy in DSP Implementations***: Number Formats for Signals and Coefficients in DSP Systems, Dynamic Range and Precision, Sources of Error in DSP Implementations-A/D Conversion Errors, DSP Computational Errors, D/A Conversion Errors	08
MODULE 2	***Architecture for Programmable DSP Devices***: Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Module, Programmability and Program Execution, Execution Control-Hardware Looping, Interrupts, Stacks, Relative Branch Support, Speed Issues, Pipelining-Pipelining and Performance, Pipeline Depth, Interlocking, Branching Effects, Interrupt Effects, Pipeline Programming Models. Features for External Interfacing	08
MODULE 3	***Programmable Digital Signal Processors***: Commercial Digital Signal-Processing Devices, The Architecture of TMS320C54XX Processors, Data Addressing Modes of TMS320C54XX Processors, Memory Space of TMS320C54XX Processors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.	08

MODULE 4	***Implementation of DSP Algorithms***: -The Q-Notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, An FFT Algorithm for DFT Computation, A Butterfly Computation-Overflow and Scaling, Bit-Reversed Index Generation, An 8-Point FFT Implementation on The TMS320C54XX, Computation of the Signal Spectrum.	08
MODULE 5	***Interfacing Memory and Peripherals to DSP Processor***: -Memory Space Organization, External Bus Interfacing Signals, Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts and I/O, Direct Memory Access (DMA). A Multichannel Buffered Serial Port (MCBSP), MCBSP Programming, A CODEC Interface Circuit, CODEC Programming, A CODEC-DSP Interface Example.	08
TEXT BOOKS	1. Singh, A. and Srinivasan, S., "*Programmable DSP Architecture and Applications"* Thomson, 2004. / Brooks/ Cole, a part of CENGAGE Learning 2004. 2. Lapsley, P. et.al, "*DSP Processor Fundamentals: Architectures and Features*", John Wiley & Sons 1996 3. Sen M. Kuo, Woon-Seng Gan "Digital Signal Processors-Architecture, Implementations and Applications", Pearson,2005.	
REFERENCE BOOKS	1. Bateman, A. and Yates, W. "*Digital Signal Processing Design"*, Computer Science Press, 1989. 2. Texas Instrument "*Digital Signal Processing Applications with the TMS320 Family*", Prentice-Hall, 1988. 3. Texas Instruments, "Linear Circuits: *Data Conversion, DSP Analog Interface, and Video Interface*", 1992	

COURSE OUTCOME

After completion of this course, students should be able to

1. Know the important basic concepts of Digital Signal Processing and the issues related to computational accuracy of algorithms when implemented using Programmable Digital Signal Processors.
2. Architectural features of programmable DSP devices based on the DSP operations these devices are generally required to perform.
3. Know the architecture and programming of programmable DSP devices (DSP320C54XX Processor).
4. Implementation of basic DSP algorithms in programmable DSP devices (DSP320C54XX Processor).
5. Interfacing memory and serial and parallel I/O peripherals to programmable DSP devices (DSP320C54XX Processor).

HIGH LEVEL VLSI DESIGN (PE-3)

COURSE OBJECTIVE

1. This course is an introduction to the HDL language. The emphasis is on writing synthesizable code and enough simulation code to write a viable test-bench.
2. This class addresses targeting Xilinx devices specifically and FPGA devices in general.
3. The information gained can be applied to any digital design by using a top-down synthesis design approach.

MODULE	CONTENTS	HOURS
MODULE 1	***Digital Design Flow***: Design Entry, Test Bench in Verilog, Design Validation, Post Synthesis Simulation, Timing Analysis, Hardware Generation; ***Verilog HDL***: Verilog Evolution, Verilog Attributes, The Verilog Language; ***Characterizing Hardware Languages***: Timing, Concurrency, Timing And Concurrency Example; ***Module Basics***: Code Format, Logic Value System, Wires And Variables, Modules, Module Ports, Names, Numbers, Arrays, Verilog Operators, Verilog Data Types, Array Indexing; ***Compiler Directives***: `Timescale, `Default Net Type, `Include, `Define.	08
MODULE 2	Abstraction Levels in VLSI Design; Adder Architectures, Multiplier Architectures, Counter Architectures, ALU Architectures. Latches, Flip-Flops, Registers and Register Files. PLA Design, Gate Array Approach, Standard Cell Approach, PLA-Based Implementation, Random Logic Implementation, Micro-Programmed Implementation (ROM-Based Implementation).	08
MODULE 3	***State Machine***: Introduction, Design Style 1, Design Style 2, ***Encoding Style***: Binary to One Hot, Moore Machine, Mealy Machine, String Detector, Traffic Light Controller.	08
MODULE 4	SRAM Cell, Different DRAM Cells, Arraying of Cells, Address Decoding, Read / Write Circuitry, Sense Amplifier Design, ROM Design.	08
MODULE 5	Clock Skew, Clock, Distribution and Routing, Clock Buffering, Clock Domains, Gated Clock, Clock Tree, Concept of Logic Hazards.	08
TEXT BOOKS	1. Z. Navabi, "*Verilog Digital System Design*", Second Edition, Tata McGraw Hill, 2008. 2. S. Palnitkar, "Verilog HDL, *A Guide to Digital Design and Synthesis*", Second Edition, Pearson Education, 2003.	
REFERENCE BOOKS	1. C. H. Roth, "*Digital Systems Design Using VHDL*", Thomson Publications, Fourth Edition, 2002.	

COURSE OUTCOME

After completion of this course, students should be able to

1. Implement the HDL portion of coding for synthesis.
2. Identify the differences between behavioral and structural coding styles efficient design of sequential circuits.
3. Understand the basic principle of circuit design and analysis.
4. Understand the sequential circuit and its synthesis.
5. Understand the RT level design and test.

RTL SIMULATION AND SYNTHESIS (PE-3)

COURSE OBJECTIVE

1. Familiarity of Finite State Machines, RTL design using reconfigurable logic.
2. Design and develop IP cores and Prototypes with performance guarantees
3. Use EDA tools like Cadence, Mentor Graphics and Xilinx.

MODULE	CONTENTS	HOURS
MODULE 1	Top Down Approach to Design, Design of FSMs (Synchronous and Asynchronous), Static Timing Analysis, Meta-Stability, Clock Issues, Need and Design Strategies for Multi-Clock Domain Designs	
MODULE 2	Design Entry by Verilog/VHDL/FSM, Verilog AMS.	
MODULE 3	Programmable Logic Devices, Introduction to ASIC Design Flow, FPGA, SOC, Floor Planning, Placement, Clock Tree Synthesis, Routing, Physical Verification, Power Analysis, ESD Protection	
MODULE 4	Design for Performance, Low Power VLSI Design Techniques. Design for Testability	
MODULE 5	IP And Prototyping: IP In Various Forms: RTL Source Code, Encrypted Source Code, Soft IP, Netlist, Physical IP, Use of External Hard IP During Prototyping. Case Studies and Speed Issues.	
TEXT BOOKS	1. Richard S. Sandige, "*Modern Digital Design*", MGH, International Editions. 2. Donald D Givone, "Digital Principles and Design", TMH 3. Charles Roth, Jr. And Lizy K John, "*Digital System Design Using VHDL*", Cengage Learning.	
REFERENCE BOOKS	1. Samir Palnitkar, "*Verilog HDL, A Guide to Digital Design and Synthesis*", Prentice Hall. 2. Doug Amos, Austin Lesea, Rene Richter, "*FPGA Based Prototyping Methodology Manual*", Xilinx 3. Bob Zeidman, "*Designing with FPGAs & CPLDs*", CMP Books.	

COURSE OUTCOME

After completion of this course, students should be able to

1. Learn top down approach to design.
2. Understand design entry by different HDL.
3. Learn the ASIC design flow.
4. Know the low power VLSI design techniques.
5. Gather knowledge on IP.

CAD OF DIGITAL SYSTEMS (PE-3)

COURSE OBJECTIVE

1. Fundamentals of CAD tools for modelling, design, test and verification of VLSI systems.
2. Study of various phases of CAD, including simulation, physical design, test and verification.
3. Demonstrate knowledge of computational algorithms and tools for CAD.

MODULE	CONTENTS	HOURS
MODULE 1	Introduction to VLSI Methodologies – Design and Fabrication of VLSI Devices, Fabrication Process and its Impact on Design	08
MODULE 2	VLSI Design Automation Tools – Data Structures and Basic Algorithms, Graph Theory and Computational Complexity, Tractable and Intractable Problems.	08
MODULE 3	General Purpose Methods for Combinational Optimization – Partitioning, Floor Planning and Pin Assignment, Placement, Routing.	08
MODULE 4	Simulation – Logic Synthesis, Verification, High Level Synthesis.	08
MODULE 5	MCMS-VHDL-Verilog-Implementation of Simple Circuits Using VHDL	08
TEXT BOOKS	1. N.A. Sherwani, "*Algorithms for VLSI Physical Design Automation*".	
REFERENCE BOOKS	2. S.H. Gerez, "*Algorithms for VLSI Design Automation*".	

COURSE OUTCOME

After completion of this course, students should be able to

1. Know VLSI design methodologies.
2. Learn VLSI automation tools.
3. Learn about physical design methods of VLSI.
4. Understand the synthesis process in VLSI.
5. Implementation of simple circuits using HDL.

VLSI DESIGN VERIFICATION & TESTING (PE-4)

COURSE OBJECTIVE:

1. To expose the students, the basics of testing techniques for VLSI circuits and Test Economics.
2. Tackle the problems associated with testing of semiconductor circuits at earlier design levels so as to significantly reduce the testing costs.
3. Identify the design for testability methods for combinational & sequential CMOS circuits.

MODULE	CONTENT	HOURS
MODULE 1	***Verilog For Verification***: Language Introduction, Levels of Abstraction, Module, Ports Types And Declarations, Registers And Nets, Arrays, Identifiers, Parameters, Relational, Arithmetic, Logical, Bitwise Shift Operators, Writing Expressions, Behavioural Modelling, Structural Coding, Continuous Assignments, Procedural Statements, Always, Initial Blocks, Begin End, Fork Join, Blocking And Non-	8

	Blocking Statements, Operation Control Statements, If, Case, Loops: While, For-Loop, For-Each, Repeat, Combination And Sequential Circuit Designs, Memory Modelling, State Machines, Writing Tasks, Writing Functions, System Tasks, Delays, Specify Block.	
MODULE 2	***Verification Methodologies***: Directed Vs Random, Functional Verification Process, Stimulus Generation, Bus Function Model, Monitors and Reference Model, Coverage Driven Verification, Verification Planning and Management. ***Introduction to System Verilog***: Datatypes, Structure & Unions, Arrays, Queues, Events, Fork-Join, Semaphore, Mailbox. OOP Concept: OOP Basics, Classes – Objects and Handles, Polymorphism and Inheritance, Encapsulation, Abstract/Parameterized/Nested Class, Casting – Static & Dynamic, Copy – Deep Copy, Shallow Copy, Scope Resolution Operator, This & Null, Typedef Class, Pure Class.	8
MODULE 3	***Randomization***: Constraint Random Verification, Randomizing Objects/Variables/Methods, Constraint Block, Inline Constraint, Global Constraint, Constraint Mode, Constraint Expressions, ***Rand Case System Verilog - Threads and Virtual Interfaces:*** Fork Join, Event Control Mailboxes and Semaphores, Interfaces	8
MODULE 4	***Coverage***: Functional Coverage- Introduction, Cover Group, Cover Point, Cover Point Expression, Coverage Bins – Explicit Bins, Transition Bins, Wildcard Bins, Ignore Bins, Illegal Bins, Cross Coverage, Coverage Options Coverage Methods Code Coverage: Statement Coverage, Branch Coverage, Expression Coverage Path Coverage, Toggle Coverages – State, Arc and Sequence Coverage	8
MODULE 5	***Assertion Based Verification – System Verilog Assertion***: Introduction to Assertion Based Verification, Immediate Assertions, Concurrent Assertions Sequences& Properties, Multi Clock Support, Advanced SVA Features Assertion Coverage	8
TEXT BOOK	1. Spear, C. (2008). "System *Verilog For Verification: A Guide to Learning the Testbench Language Features",* Springer Science & Business Media. 2. Vijayaraghavan, S., & Ramanathan, M. (2005). "*A Practical Guide for System Verilog Assertions",* Springer Science & Business Media.	
REFERENCE BOOK	*1. System Verilog 3.1a Language Reference Manual.* 2. Bergeron, J., Cerny, E., Hunter, A., & Nightingale, A. (2006). *"Verification Methodology Manual for System Verilog",* Springer Science & Business Media. 3. Bergeron, J. (2007). "*Writing Testbenches Using System Verilog"*. Springer Science & Business Media.	
COURSE OUTCOME: After completion of course, student should be able to 1. Familiarity of front-end design and verification techniques and create reusable test environments. 2. Verify increasingly complex designs more efficiently and effectively. 3. Use EDA tools like Cadence, Mentor Graphics.		

4. Acquire knowledge about fault modeling and collapsing.
5. Learn about various combinational ATPG and sequence pattern generation.

LOW POWER VLSI DESIGN (PE-4)

COURSE OBJECTIVE

1. Study of sources of power dissipation in digital IC systems
2. Study of model power consumption & understand the basic analysis methods.
3. Study of leakage sources and reduction techniques.

MODULE	CONTENTS	HOURS
MODULE 1	***Technology & Circuit Design Levels***: Sources of Power Dissipation in Digital ICs, Degree of Freedom, Recurring Themes in Low-Power, Emerging Low Power Approaches, Dynamic Dissipation In CMOS, Effects of V_{DD} & V_T on Speed, Constraints on V_T Reduction, Transistor Sizing & Optimal Gate Oxide Thickness, Impact of Technology Scaling, Technology Innovations.	08
MODULE 2	***Low Power Circuit Techniques***: Power Consumption in Circuits, Flip-Flops & Latches, High Capacitance Nodes, Energy Recovery, Reversible Pipelines, High Performance Approaches.	08
MODULE 3	***Low Power Clock Distribution***: Power Dissipation in Clock Distribution, Single Driver Versus Distributed Buffers, Buffers & Device Sizing Under Process Variations, Zero Skew Vs. Tolerable Skew, Chip & Package Co-Design of Clock Network.	08
MODULE 4	***Logic Synthesis for Low Power Estimation Techniques***: Power Minimization Techniques, Low Power Arithmetic Components-Circuit Design Styles, Adders, Multipliers.	08
MODULE 5	***Low Power Memory Design***: Sources & Reduction of Power Dissipation in Memory Subsystem, Sources of Power Dissipation In DRAM & RAM, Low Power DRAM Circuits, Low Power SRAM Circuits. ***Low Power Microprocessor Design System***: Power Management Support, Architectural Trade-Offs for Power, Choosing the Supply Voltage, Low-Power Clocking, Implementation Problem for Low Power, Comparison of Microprocessors for Power & Performance	08
TEXT BOOKS	1. P. Rashinkar, Paterson and L. Singh, "*Low Power Design Methodologies*", Kluwer Academic, 2002 2. Kaushik Roy, Sharat Prasad, "*Low Power CMOS VLSI Circuit Design*", John Wiley sons Inc.,2000. 3. Gary Yeap, "*Practical Low Power Digital VLSI Design*", Kluwer, 1998.	
REFERENCE BOOKS	1. Rabaey, Pedram, *Low power design methodologies,* Kluwer Academic, 1997 2. W. Nebel and J. Mermet, *Low Power Design in Deep Sub-micron Electronics,* Kluwer Academic Publishers, 1997	

	3. B.Kulo and J.H Lou, "*Low voltage CMOS VLSI Circuits*", Wiley, 1999. 4. A.P.Chandrasekaran and R.W.Broadersen, "*Low Power Digital CMOS Design*", Kluwer,1995

COURSE OUTCOME

After completion of this course, students should be able to

1. Identify the sources of power dissipation in digital IC systems & understand the impact of power on system performance and reliability.
2. Understand various techniques for low power circuit design.
3. Know clock distribution for low power circuits.
4. Learn Power Minimization Techniques of Logic Synthesis for Low Power Estimation Techniques.
5. How to design Low power memory and Microprocessor systems.

DESIGN WITH ASICS (PE-4)

COURSE OBJECTIVE

1. Study design methodologies of ASIC.
2. Study of various FPGA families.
3. Case studies of electronic gadgets

MODULE	CONTENTS	HOURS
MODULE 1	Types of ASICs. ASIC Design Flow. Programmable ASICs. Anti-Fuse, SRAM, EPROM, EEPROM Based ASICs. Programmable ASIC Logic Cells and I/O Cells. Programmable Interconnects. An Overview of Advanced FPGAs and Programmable SOCs: Architecture and Configuration of Spartan and Virtex FPGAs. Apex and Cyclone FPGAs. Virtex PRO Kits and Nios Kits. OMAP	10
MODULE 2	ASIC Physical Design Issues. System Partitioning, Interconnect Delay Models and Measurement of Delay. ASIC Floor Planning, Placement and Routing.	08
MODULE 3	Design Issues in SOC. Design Methodologies. Processes and Flows. Embedded Software Development for SOC. Techniques for SOC Testing. Configurable SOC. Hardware/Software Co-design. High Performance Algorithms for ASICs/ SOCs.	08
MODULE 4	SOC Case Studies- DAA and Computation of FFT and DCT. High Performance Filters Using Delta-Sigma Modulators.	08
MODULE 5	SOC Case Studies: Digital Camera, Bluetooth Radio/Modem, SDRAM and USB Controllers.	06
TEXT BOOKS	1. M.J.S. Smith, *"Application Specific Integrated Circuits",* Pearson, 2003	
REFERENCE BOOKS	1. K.K. Parhi, *"VLSI Digital Signal Processing Systems",* John-Wiley, 1999	

COURSE OUTCOME

After completion of this course, students should be able to

1. About different ASIC and FPGAs.
2. Have knowledge about design issues of ASIC.

3. Learn about SOC.
4. Compute FFT and DCT.
5. Familiar with SOC applications.

VLSI DESIGN LABORATORY-II (Lab-3)

SESSIONAL OBJECTIVE

1. Familiar with digital VLSI circuits using software.
2. Analyze various types of VLSI modelling techniques.
3. Use of different FPGA boards.

No.	CONTENTS
1	Design, Simulation and FPGA Implementation of Arithmetic Circuits.
2	Design, Simulation and FPGA Implementation of Encoder and Decoder Circuit.
3	Design, Simulation and FPGA Implementation of Counters.
4	Design, Simulation and FPGA Implementation of a Simple Microprocessor Data Path.
5	Design, Simulation and FPGA Implementation of a Simple Microprocessor Control Path.
6	Design, Simulation and FPGA Implementation of Memory.

VLSI SIGNAL PROCESSING LABORATORY (Lab-4)

SESSIONAL OBJECTIVE

1. Study of advanced simulation methods.
2. Analyze Higher Order Statistics.
3. To perform the spectrum estimation

No.	CONTENTS
1	Decomposition using Multi Resolution Techniques.
2	Wavelet Coding Techniques
3	Spectral Estimation Using Parametric Method
4	Higher Order Statistics of a Signal
5	PCA/ICA Analysis

RF IC (PE-5)

COURSE OBJECTIVE:

1. To educate students fundamental RF circuit and system design skills.
2. To introduce students, the basic RF electronics utilized in the industry and how to build up a complex RF system from basics.
3. To offer students experience on designing and simulating RF circuits in computer.

MODULE	CONTENTS	HOURS
MODULE 1	Introduction, Basic Concepts in RF Design, Passive RLC Networks, Passive IC Components and Their Characteristics.	6
MODULE 2	Voltage references & biasing, Feedback Systems, Noise, Phase	8

	Noise.	
MODULE 3	High frequency amplifier design, LNA design, RF power amplifier	10
MODULE 4	Oscillators, PLL, Synthesizers, Mixers.	12
MODULE 5	Transceiver Architecture and Practical Design Example	4
TEXT BOOKS	1. T. H. Lee, "*The Design of CMOS RF Integrated Circuits*", Cambridge University Press. 2. B. Razavi, "RF *Microelectronics*", Pearson Education.	
REFERENCE BOOKS	1. B. Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw-Hill, 2002. 2. Sorin Voinigescu, "*High Frequency Integrated Circuits*", Cambridge University Press. 3. Reinhold Ludwig, Gene Bogdanov, "RF Circuit Design Theory and Applications", Pearson Education.	
COURSE OUTCOME: After completion of course, student should be able to 1. Be conversant with RF design concepts, passive on-chip elements. 2. Understand biasing, feedback and noise. 3. Design a RF amplifier, Power amplifier, LNA. 4. Be proficient with frequency conversion and signal generation. 5. 5. Present the different transceiver architecture.		

FPGA BASED DSP DESIGN (PE-5)

COURSE OBJECTIVE 1. Study of multitone modulation. 2. Brief idea about software radio. 3. Study of Speech Coding Using Linear Prediction		
MODULE	CONTENTS	HOURS
MODULE 1	Multirate Signal Processing- Decimation and Interpolation, Spectrum of Decimated and Interpolated Signals, Polyphase Decomposition of FIR Filters and Its Applications to Multidate DSP. Sampling Rate Converters, Sub-Band Encoder. Filter Banks-Uniform Filter Bank. Direct and DFT Approaches.	08
MODULE 2	Introduction to ADSL Modem, Discrete Multitone Modulation and Its Realization Using DFT. QMF. Short Time Fourier Transform Computation of DWT Using Filter Banks. Implementation and Verification on FPGAs. DDFS- ROM LUT Approach. Spurious Signals Jitter.	08
MODULE 3	Block Diagram of A Software Radio. Digital Down Converters and Demodulators. CORDIC Architectures. Universal Modulator and Demodulator Using CORDIC. Computation of Special Functions Using CORDIC. Vector and Rotation Mode Of CORDIC. Implementation and Verification on FPGAs	08

MODULE 4	Incoherent Demodulation - Digital Approach for I And Q Generation, Special Sampling Schemes. CIC Filters. Residue Number System and High-Speed Filters Using RNS. Down Conversion Using Discrete Hilbert Transform. Under Sampling Receivers, Coherent Demodulation Schemes.	08
MODULE 5	Speech Coding- Speech Apparatus. Models of Vocal Tract. Speech Coding Using Linear Prediction. CELP Coder. An Overview of Waveform Coding. Vocoders. Vocoder Attributes. Block Diagrams of Encoders and Decoders of G723.1, G726, G727, G728 And G729.	08
TEXT BOOKS	1. J. H. Reed, *Software Radio*, Pearson, 2002. 2. U. Meyer – Baese, "*Digital Signal Processing with FPGAs"*, Springer, 2004	
REFERENCE BOOKS	1. Tsui, "*Digital Techniques for Wideband receivers"*, Artech House, 2001. 2. S. K. Mitra, "*Digital Signal Processing"*, McGraw Hill, 1998	

COURSE OUTCOME

After completion of this course, students should be able to

1. Learn multirate processing.
2. Design the modem.
3. Learn CORDIC architecture.
4. Design high speed filters using redundant number system.
5. Understand the basics of speech coding.

PHYSICAL DESIGN AUTOMATION (PE-5)

COURSE OBJECTIVE

1. This course focuses on various design automation problems in the physical design process of VLSI circuits, including: logic partitioning, floor planning, placement, global routing, detailed routing, clock and power routing, and new trends in physical design.
2. To impart knowledge on implementation of graph theory in VLSI.
3. To impart knowledge on automation methods for VLSI physical design.

MODULE	CONTENT	HOURS
MODULE 1	***Preliminaries:*** Introduction to Design Methodologies, Design Automation Tools, Algorithmic Graph Theory, Computational Complexity, Tractable and Intractable Problems. ***General Purpose Methods for Combinational Optimization***: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu Search, Genetic Algorithms.	08
MODULE 2	Layout Compaction, Placement, Floor Planning and Routing Problems, Concepts and Algorithms. ***Modeling and Simulation***: Gate Level Modeling and Simulation, Switch Level Modeling and Simulation.	08

MODULE 3	***Logic Synthesis and Verification***: Basic Issues and Terminology, Binary-Decision Diagrams, Two-Level Logic Synthesis. ***High-Level Synthesis***: Hardware Models, Internal Representation of The Input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some Aspects of Assignment Problem, High-Level Transformations.	08
MODULE 4	***Physical Design Automation of FPGAs***: FPGA Technologies, Physical Design Cycle for FPGAs, Partitioning and Routing for Segmented and Staggered Models. ***Physical Design Automation of MCMs***: MCM Technologies, MCM Physical Design Cycle, Partitioning,	08
MODULE 5	Placement - Chip Array Based and Full Custom Approaches, Routing – Maze Routing, Multiple Stage Routing, Topologic Routing, Integrated Pin –Distribution and Routing, Routing and Programmable MCMs.	08
TEXT BOOKS	1. Naveed Shewani, "*Algorithms for VLSI Physical Design Automation*", Kluwer Academic, 1993 2. S.H. Gerez, "*Algorithms for VLSI Design Automation*", John Wiley, 1998.	
REFERENCE BOOKS	1. S.M. Sait & H. Youssef, "*VLSI Physical Design Automation*", World Scientific, 1999. 2. M. Sarrafzadeh, "*Introduction to VLSI Physical Design*", McGraw Hill (IE).	

COURSE OUTCOME

After completion of this course, students should be able to

1. Learn General Purpose Methods for Combinational Optimization.
2. Learn techniques of modelling and simulation at different abstraction levels.
3. Analyze physical design problems and Employ appropriate automation algorithms for Synthesis.
4. Decompose large mapping problem into pieces, including logic optimization with partitioning, placement and routing.
5. Know how to place the blocks and how to partition the blocks while for designing the layout for IC.

SIGNAL PROCESSING (OE)

COURSE OBJECTIVE

1. To explore the filter design and characterization techniques
2. To analyze multirate DSP systems.
3. To know the concept of optimum linear filters
4. To analyze the power spectrum estimation methods
5. To explore the model of adaptive filters

MODULE	CONTENTS	HOURS
MODULE 1	Overview of DSP, Characterization in Time and Frequency, FFT Algorithms, Digital Filter Design and Structures: Basic FIR/IIR Filter Design & Structures, Design Techniques of Linear Phase FIR Filters, IIR Filters by Impulse Invariance, Bilinear Transformation, FIR/IIR Cascaded Lattice Structures, And Parallel All Pass Realization Of IIR.	8
MODULE 2	Multi Rate DSP, Decimators and Interpolators, Sampling Rate Conversion, Multistage Decimator & Interpolator, Poly Phase Filters, QMF, Digital Filter Banks, Applications in Sub-Band Coding. Application of DSP & Multi Rate DSP, Application to Radar, Introduction to Wavelets, Application to Image Processing, Design of Phase Shifters, DSP In Speech Processing & Other Applications	8
MODULE 3	Linear Prediction & Optimum Linear Filters, Stationary Random Process, Forward-Backward Linear Prediction Filters, Solution of Normal Equations, AR Lattice and ARMA Lattice-Ladder Filters, Wiener Filters for Filtering and Prediction.	8
MODULE 4	Estimation of Spectra from Finite-Duration Observations of Signals. Nonparametric Methods for Power Spectrum Estimation, Parametric Methods for Power Spectrum Estimation, Minimum Variance Spectral Estimation, Eigen Analysis Algorithms for Spectrum Estimation.	8
MODULE 5	Adaptive Filters, Applications, Gradient Adaptive Lattice, Minimum Mean Square Criterion, LMS Algorithm, Recursive Least Square Algorithm.	8
TEXT BOOKS	1. J.G. Proakis and D.G. Manolakis, "*Digital Signal Processing*", Third Edition, Prentice Hall. 2. B. Widrow and Stern, "Adaptive Signal Processing".	
REFERENCE BOOKS	1. Sanjit K Mitra, "*Digital Signal Processing*", New edition, TMH. 2. Digital Signal Processing, by Salivahanan, New edition, TMH. 3. N. J. Fliege, "*Multirate Digital Signal Processing: Multirate Systems - Filter Banks – Wavelets*", 1st Edition, John Wiley and Sons Ltd, 1999. 4. S. Haykin , "*Adaptive Filter Theory*", 4th Edition, Prentice Hall, 2001.	

COURSE OUTCOME: After completion of course, student should be able to

1. Design and analyze the DSP signals and systems
2. Design efficient filters for sampling rate conversion for different applications
3. Appreciate the significance of normal equations in linear optimum filters and techniques used to solve them
4. Estimate the spectrum of signals from finite-duration observation of signals
5. Design adaptive filter models for different signal processing applications

BASICS OF VLSI ENGINEERING (OE)

COURSE OBJECTIVE

1. Study of basic design procedure of digital MOS circuits.
2. Writing VHDL code for digital circuits.
3. Writing Verilog code for digital circuits.

MODULE	CONTENTS	HOURS
MODULE 1	***VLSI Basics. - VLSI – Digital. System***: VLSI Design Flow, Y Chart, Design Hierarchy Structural. ***VLSI – FPGA Technology***: FPGA – Introduction, Gate Array Design, Standard Cell Based Design, Full Custom Design.	06
MODULE 2	***VLSI MOS Transistor***: Structure of a MOSFET, Working of a MOSFET, MOSFET Current – Voltage Characteristics. ***VLSI – MOS Inverter:*** Principle of Operation, Resistive Load Inverter, Inverter with N type MOSFET Load, Enhancement Load NMOS, Depletion Load NMOS, CMOS Inverter – Circuit, Operation and Description	06
MODULE 3	***VLSI – Combinational MOS Logic Circuits***: CMOS Logic Circuits, Complex Logic Circuits, Complex CMOS Logic Gates, ***VLSI – Sequential MOS Logic Circuits***: CMOS Logic Circuits, CMOS Logic Circuits.	08
MODULE 4	***VHDL – Introduction***: Data Flow Modeling, Behavioral Modeling, Structural Modeling, Logic Operation – AND GATE, Logic Operation – OR Gate, Logic Operation – NOT Gate, Logic Operation – NAND Gate, Logic Operation – NOR Gate, Logic Operation – XOR Gate, Logic Operation – X-NOR Gate, ***VHDL – Programming for Combinational Circuits:*** VHDL Code for a Half-Adder, VHDL Code for a Full Adder, VHDL Code for a Half-Subtractor, VHDL Code for a Full Subtractor, VHDL Code for a Multiplexer, VHDL Code for a Demultiplexer, VHDL Code for a 8 x 3 Encoder, VHDL Code for a 3 x 8 Decoder, VHDL Code – 4 bit Parallel adder, VHDL Code – 4 bit Parity Checker, VHDL Code – 4 bit Parity Generator, ***VHDL – Programming for Sequential Circuits*** ; VHDL Code for an SR Latch, VHDL Code for a D Latch, VHDL Code for an SR Flip Flop, VHDL code for a JK Flip Flop, VHDL Code for a D Flip Flop, VHDL Code for a T Flip Flop, VHDL Code for a 4 - bit Up Counter, VHDL Code for a 4-bit Down Counter.	10
MODULE 5	***Verilog – Introduction***: Behavioral level, Register−Transfer Level, Gate Level, Lexical Tokens, Gate Level Modelling, Data Types, Operators, Operands, Modules, ***Verilog – Behavioral Modelling & Timing Control***: Procedural Assignments, Delay in Assignment (not for synthesis), Blocking Assignments, Nonblocking (RTL) Assignments, Conditions, Delay Controls, Procedures: Always and Initial Blocks.	10
TEXT BOOKS	1. Kang, Sung-Mo, and Yusuf Leblebici. "*CMOS Digital Integrated Circuits*", Tata McGraw-Hill Education, 2003.	

	2. S. Palnitkar, "*Verilog HDL, A Guide to Digital Design and Synthesis*", Second Edition, Pearson Education, 2003. 3. Volnei A. Pedroni, "*Circuit Design with VHDL*", PHI, 2005.
REFERENCE BOOKS	1. N.H.E. Weste a n d D.M. Harris, "*MOS VLSI d e s i g n : A Circuits and Systems Perspective*", 4th Edition, Pearson Education India, 2011 3. Z. Navabi, "*Verilog Digital System Design*", Second Edition, Tata McGraw Hill, 2008. 3.Douglas L. Perry, "*VHDL: Programming by Example*", 4th Edition, Tata McGraw Hill, 2004.
COURSE OUTCOME After completion of this course, students should be able to 1. Understand basics of VLSI circuits and systems. 2. Understand basic principles of MOS transistor and MOS inverters. 3. Design combinational as well as sequential logic circuits. 4. Write VHDL programming for logic circuits. 5. Write Verilog programming for logic circuits	

AUDIO & VIDEO SYSTEMS (OE)

COURSE OBJECTIVE

1. To study characteristics of sound and audio devices.
2. To study characteristics of digital television.

To know the display systems

MODULE	CONTENTS	HOURS
MODULE 1	***Characteristics of Sound***: Nature of Sound, Pressure and Intensity of Sound Waves, Sensitivity of Human Ear for Sound, Frequency of Sound Waves, Overtones and Timbre, Intervals Octaves and Harmonics, Pitch, Resonance Effect in Sound Systems, Helmholtz Resonator, Reflection and Diffraction of Sound Waves. ***Audio Devices and Their Applications***: Microphones, Loudspeakers.	
MODULE 2	***Loudspeaker***: Column or Line Source Speakers, Baffles and Enclosures, Multi-Way Speaker System (Woofers and Tweeters), Consequence of Mismatch Between Amplifier Output and Loudspeaker Impedance. ***Optical Recording***: Types of Optical Recording of Sound, Methods of Optical Recording of Sound on Film, Reproduction of Sound from Films, Modern Method of Recording of Sound for Movie Films, Compact Disc, Optical Recording on Disc, Playback Process, Comparison of Compact Discs and Conventional (Gramophone) Discs. Introduction to Blue Ray Technology, Introduction to High Fidelity (Hi-Fi) Systems, Introduction to Public Address Systems (PA-Systems), Introduction to Audio Amplifiers, Introduction to Acoustic Reverberation, Introduction to AM/FM Tuners, Introduction to USB MP3 Players.	

MODULE 3	***Television Fundamentals***: Elements of TV Communication System, Scanning, Synchronization, Aspect Ratio, Pixels, Resolution, Bandwidth, Composite Video Signal, Modulation of Video and Audio Signals, Monochrome and Color Cameras, Compatibility, Luminance and Chrominance Signal, Picture Tubes, Solid State Picture Transducers, TV Broadcasting Systems, Video Monitors. ***Digital Television-Transmission and Reception***: Digital System Hardware, Signal Quantizing and Encoding, Digital Satellite Television, Direct-To-Home (DTH) Satellite Television, Digital TV Receiver, Merits of Digital TV Receivers, Digital Terrestrial Television (DTT), Introduction to Video on Demand, Introduction To CCTV, Introduction To CATV.	
MODULE 4	Stereophonic Sound, Flat Panel TV Receivers, 3-Dimensional TV, EDTV, ***HDTV And Digital Studio Equipment***: Stereo Sound Systems, Projection Television, Flat Panel Display TV Receivers, Three Dimensional (3-D) Television, Advances In 3D TV Technology, Present Status Of New 3D Receivers, Extended Definition Television(EDTV), Digital Equipment For Television Studios, Electronic Control Of Studio Lights, Digital Audio Recorders And Editing, Colour Receivers Of New Generation, Liquid Crystal And Plasma Screen Televisions: LCD Technology, LCD Matrix Types And Operation, LCD Screens For Television, Plasma And Conduction Of Charge, Plasma Television Screens, Signal Processing In Plasma TV Receivers, A Plasma Colour Receiver, LCD Colour Receivers, Single LCD Receivers, 3-LCD Colour Receivers, Plasma Or LCD-Which Is The Best Choice, Performance Comparison Of Plasma And LCD Televisions, Introduction To LED TV, RGB Dynamic LEDs, Edge-LEDs, Differences Between LED-Backlit And Backlit LCD Displays, Comparison Of Plasma TV And LED TV, Introduction To OLED TVs	
MODULE 5	***Projection Display Systems And Television Home Theatres***: Direct View And Rear Projection Systems, Front Projection TV System, Transmittive Type Projection Systems, Reflective Projection Systems, Digital Light Processing(DLP) Projection System, Projection Television For Home Theatres, Choice Of Projection TV System, Essential Features Of Front Projectors, Comparison And Choice Of Rear Projection Receivers, Satellite Off-Air Tuners And Digital Video Recorders, Surround Sound Stereo Receiver, Top Of The Line Home Theatre.	
TEXT BOOKS	1. Modern Television Practice (Fourth revised edition) - R. R. Gulati, New Age International Publishers. 2. Audio and Video Systems (Second Edition) - R. G. Gupta, McGraw Hill Education Limited	
REFERENCE BOOKS	1. Television & Video Engineering (Second edition) - A. M. Dhake, McGraw Hill Education Limited. 2. Essential Guide to Digital Video - John Watkinson, Snell & Wilcox Inc.	

	Publication. 3. Guide to Compression - John Watkinson, Snell & Wilcox Inc. Publication Consumer Electronics - S. Bali, Pearson Education.

COURSE OUTCOME

After completion of this course, students should be able to

1. Explain importance of Digital Audio and Video systems.
2. Distinguish between Stereo & Hi-fi Amplifier
3. Understand CD/DVD player mechanism.
4. Explain AM/FM tuners, MP3 players and Blue-Ray Technology.
5. Explore advanced Digital colour Television systems.